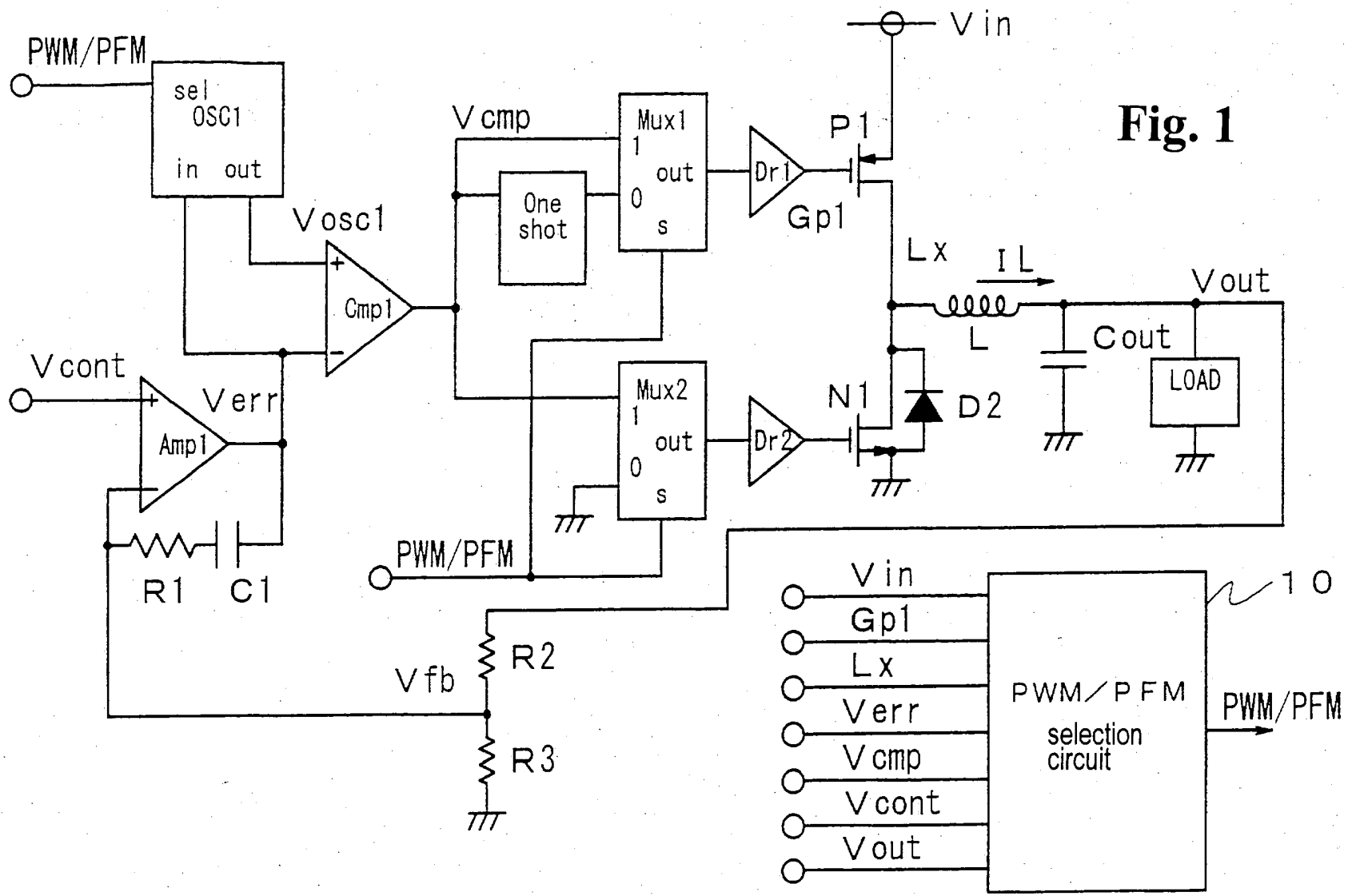

PWM/PFM
sel
OSC1
in out
Vosc1
Cmp1
Vcont
Amp1
Verr
R1
C1
Vcmp
One shot
Mux1
1
out
0
s
Mux2
1
out
0
s
PWM/PFM
Dr1
Dr2
P1
Gp1
N1
Vin
Lx
IL
L
Vout
Cout
LOAD
D2
R2
Vfb
R3
Vin
Gp1
Lx
Verr
Vcmp
Vcont
Vout
PWM／PFM
selection
circuit
10
PWM/PFM

Fig. 1

Fig. 2

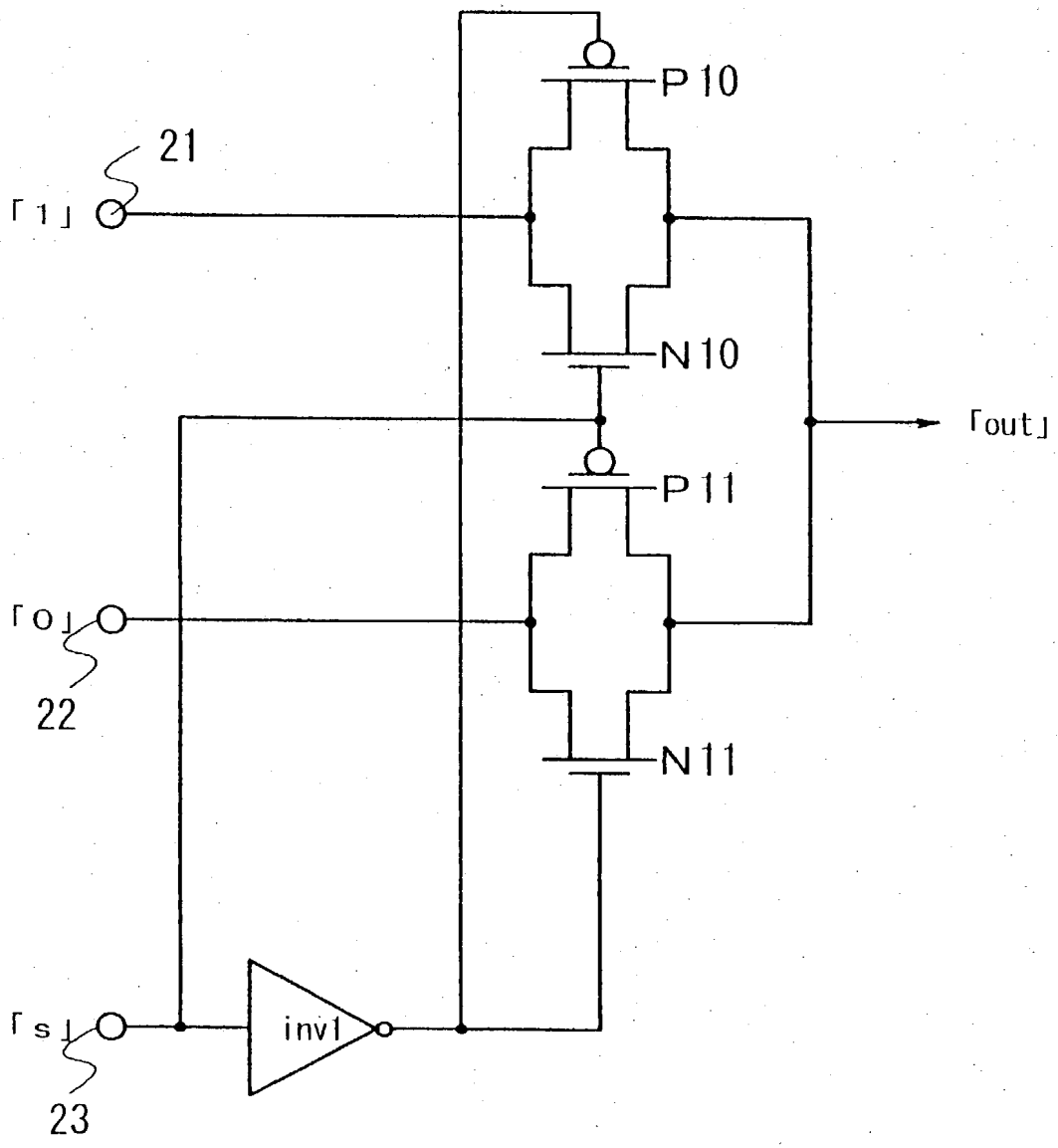


Fig. 3

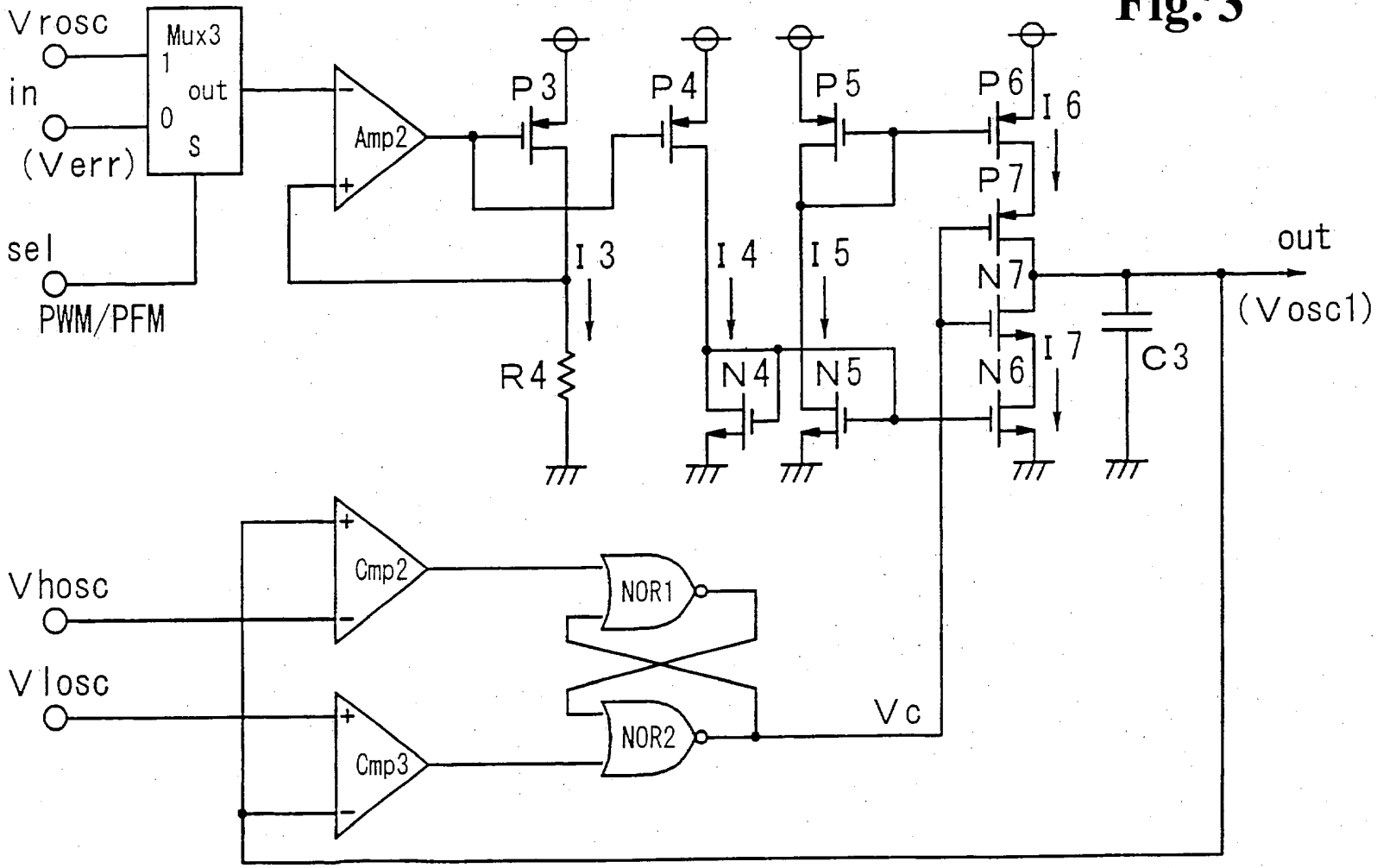

Vrosc
in
(Verr)
sel
PWM/PFM
Mux3
1
0
out
S
Amp2
P3
P4
P5
P6
P7
I6
I3
I4
I5
I7
R4
N4
N5
N6
N7
C3
out
(Vosc1)
Vhosc
Vlosc
Cmp2
Cmp3
NOR1
NOR2
Vc

Fig. 4

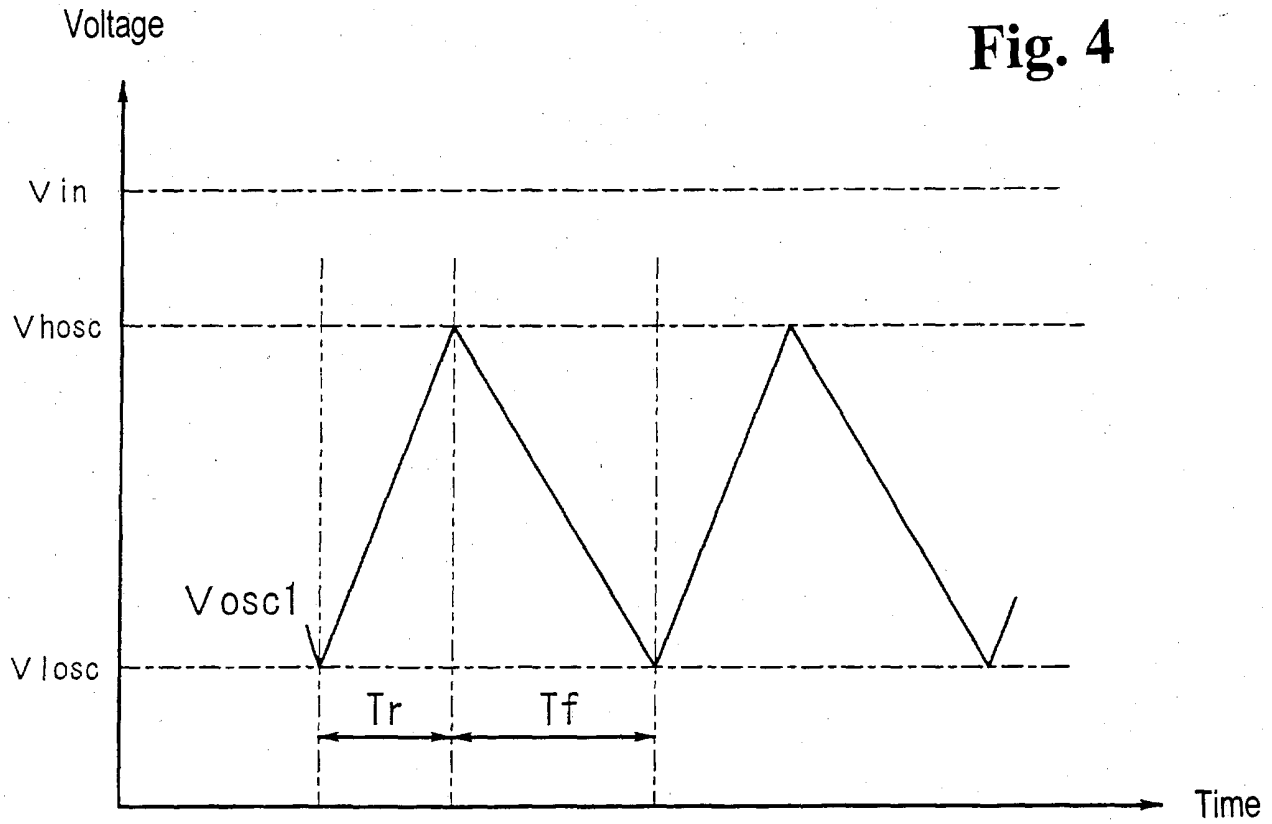


Fig. 5

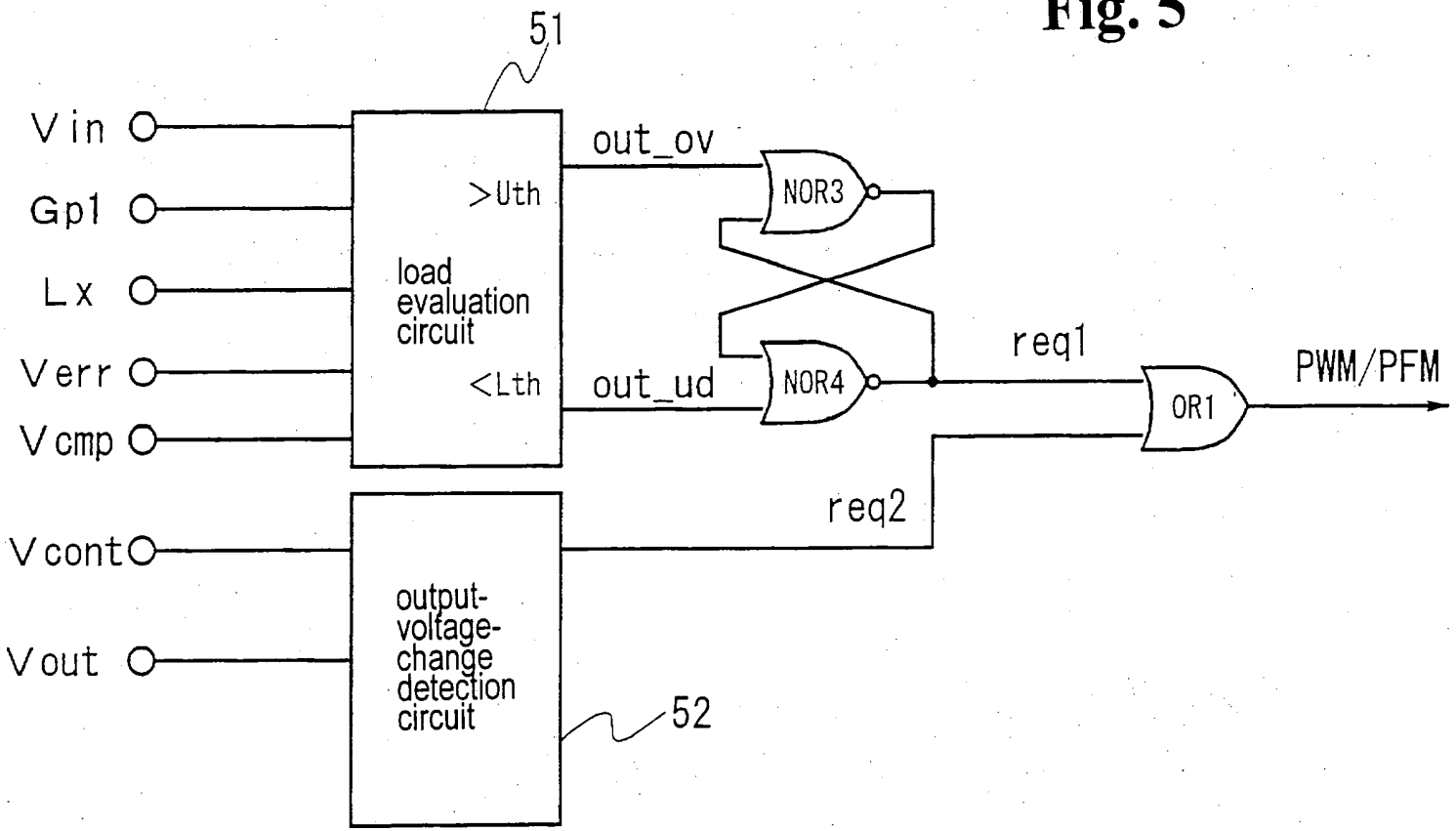
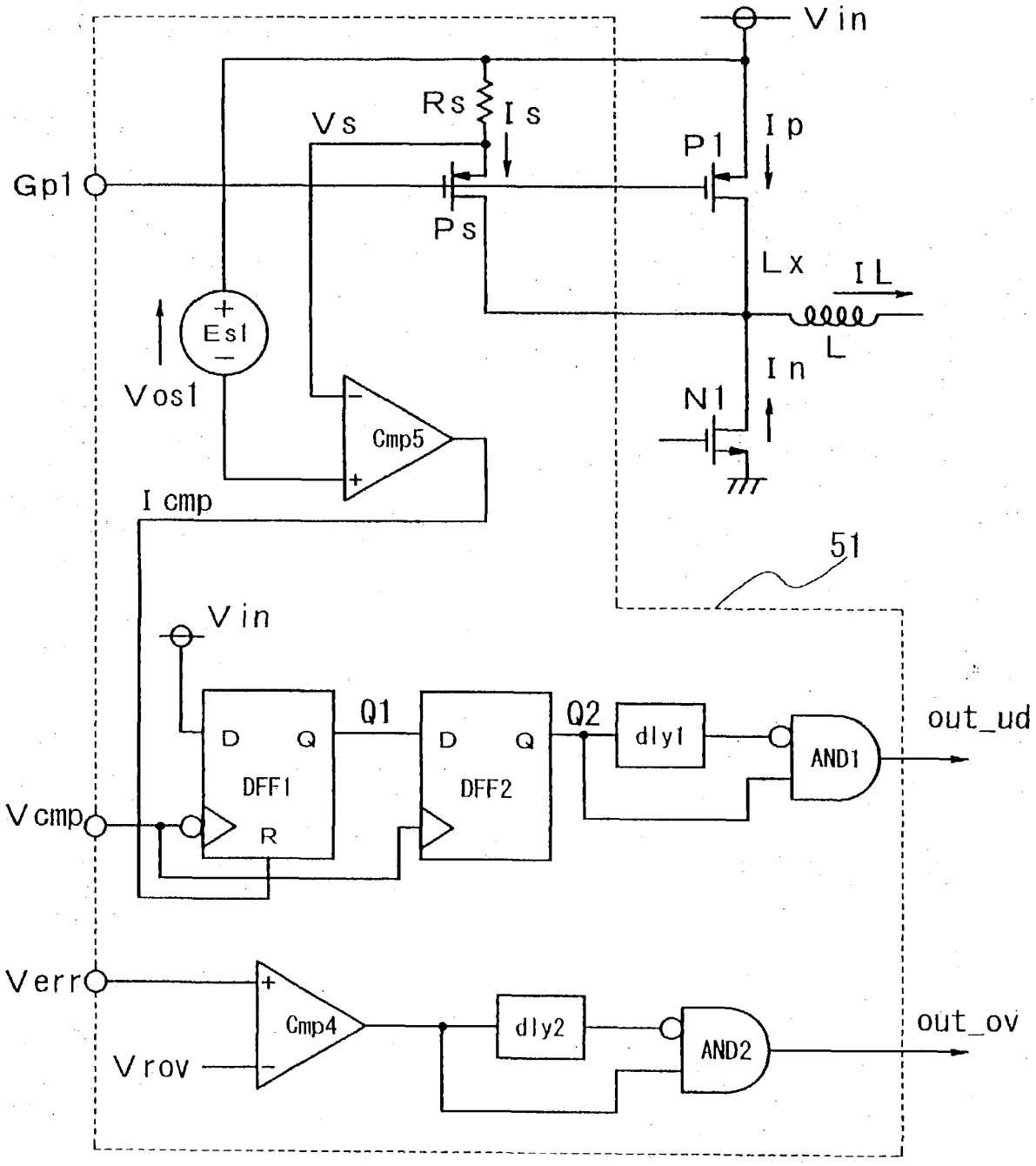

51
Vin
Gp1
Lx
Verr
Vcmp
>Uth
load evaluation circuit
<Lth
out_ov
out_ud
NOR3
NOR4
req1
OR1
PWM/PFM
req2
Vcont
Vout
output-voltage-change detection circuit
52

Fig. 6

load conditions \ output voltages	no change (req2=Low)	no change (req2=High)
light load (req1=Low)	PWM/PFM =Low	PWM/PFM =High
heavy load (req1=High)	PWM/PFM =High	PWM/PFM =High

Fig. 7


Vin
Rs
Is
Vs
Ip
P1
Gp1
Ps
Lx
IL
L
Es1
Vos1
In
N1
Cmp5
I cmp
51
Vin
D
Q
DFF1
R
Q1
D
Q
DFF2
Q2
dly1
AND1
out_ud
Vcmp
Verr
Cmp4
dly2
AND2
out_ov
Vrov

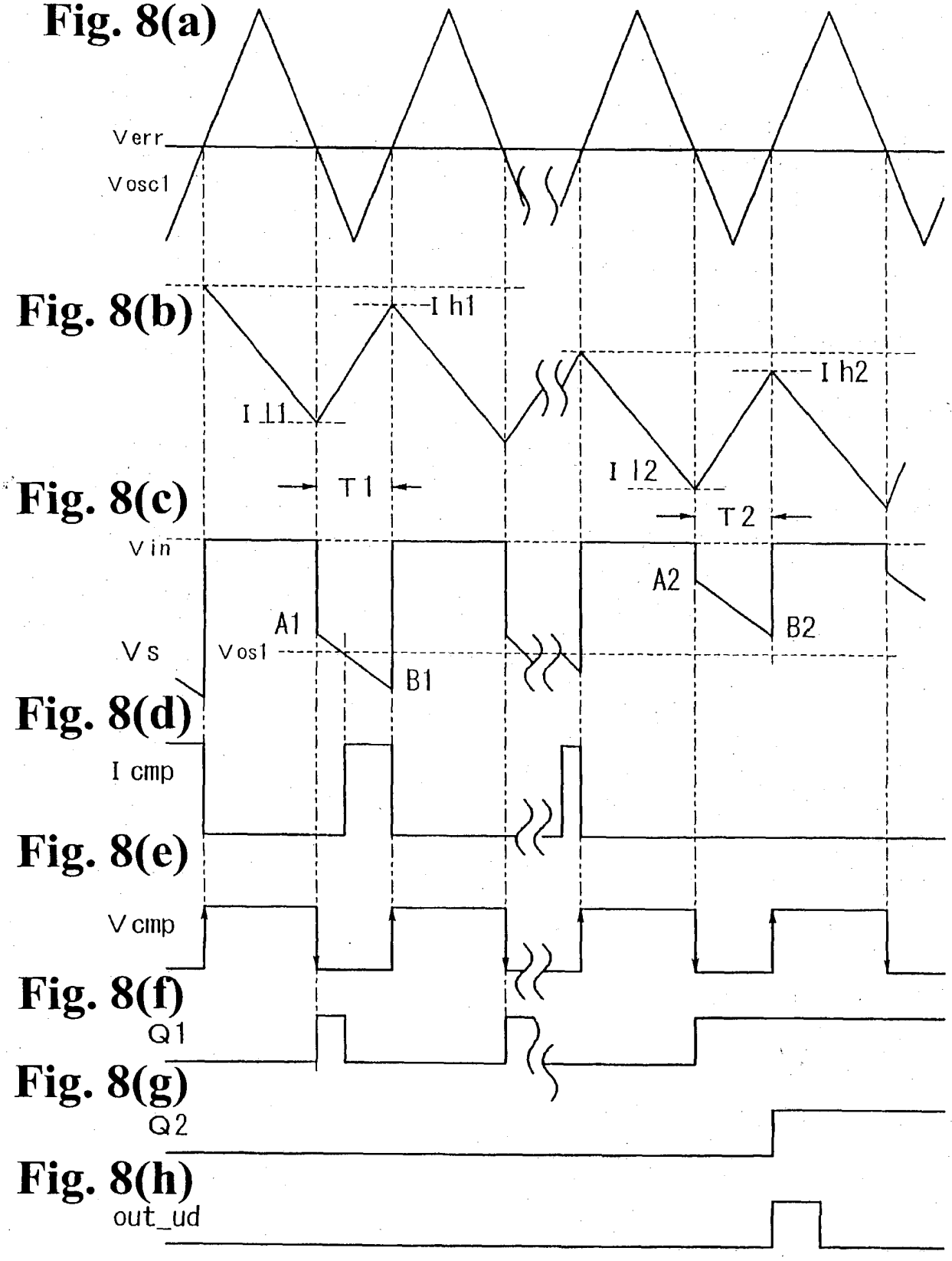


Fig. 8(a)
Verr
Vosc1
Fig. 8(b)
I h1
I h2
I l1
I l2
Fig. 8(c)
T1
T2
Vin
A1
A2
B1
B2
Vs
Vos1
Fig. 8(d)
I cmp
Fig. 8(e)
Vcmp
Fig. 8(f)
Q1
Fig. 8(g)
Q2
Fig. 8(h)
out_ud

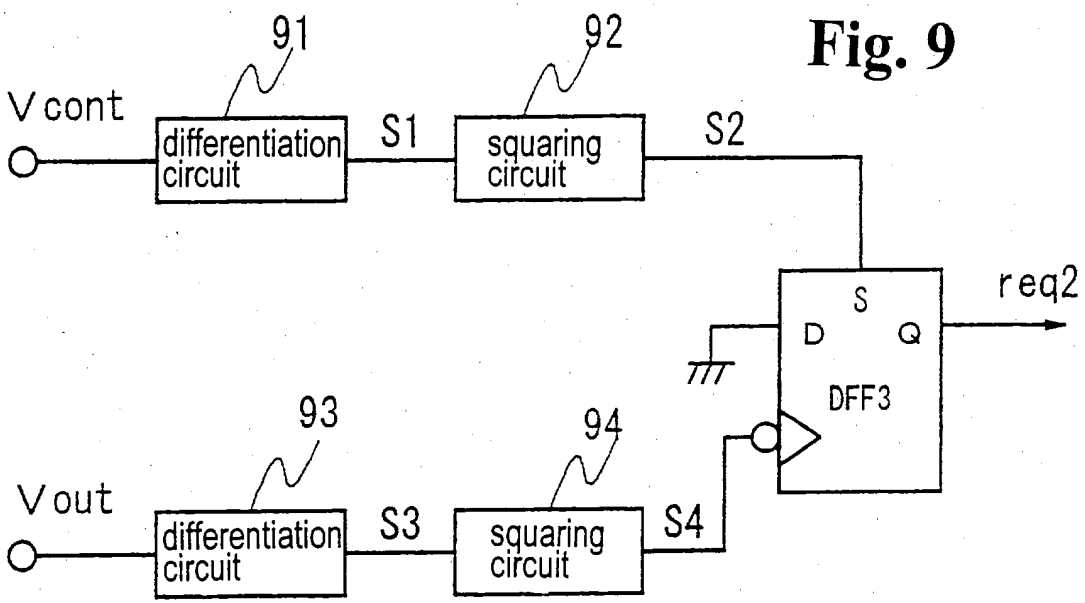

91
92
Vcont
differentiation circuit
S1
squaring circuit
S2
S
D
Q
req2
DFF3
93
94
Vout
differentiation circuit
S3
squaring circuit
S4

Fig. 9

Fig. 10(a)

Vcont

Fig. 10(b)

Vout

Fig. 10(c)

S1

Fig. 10(d)

S2

Fig. 10(e)

S3

Fig. 10(f)

S4

Fig. 10(g)

req2

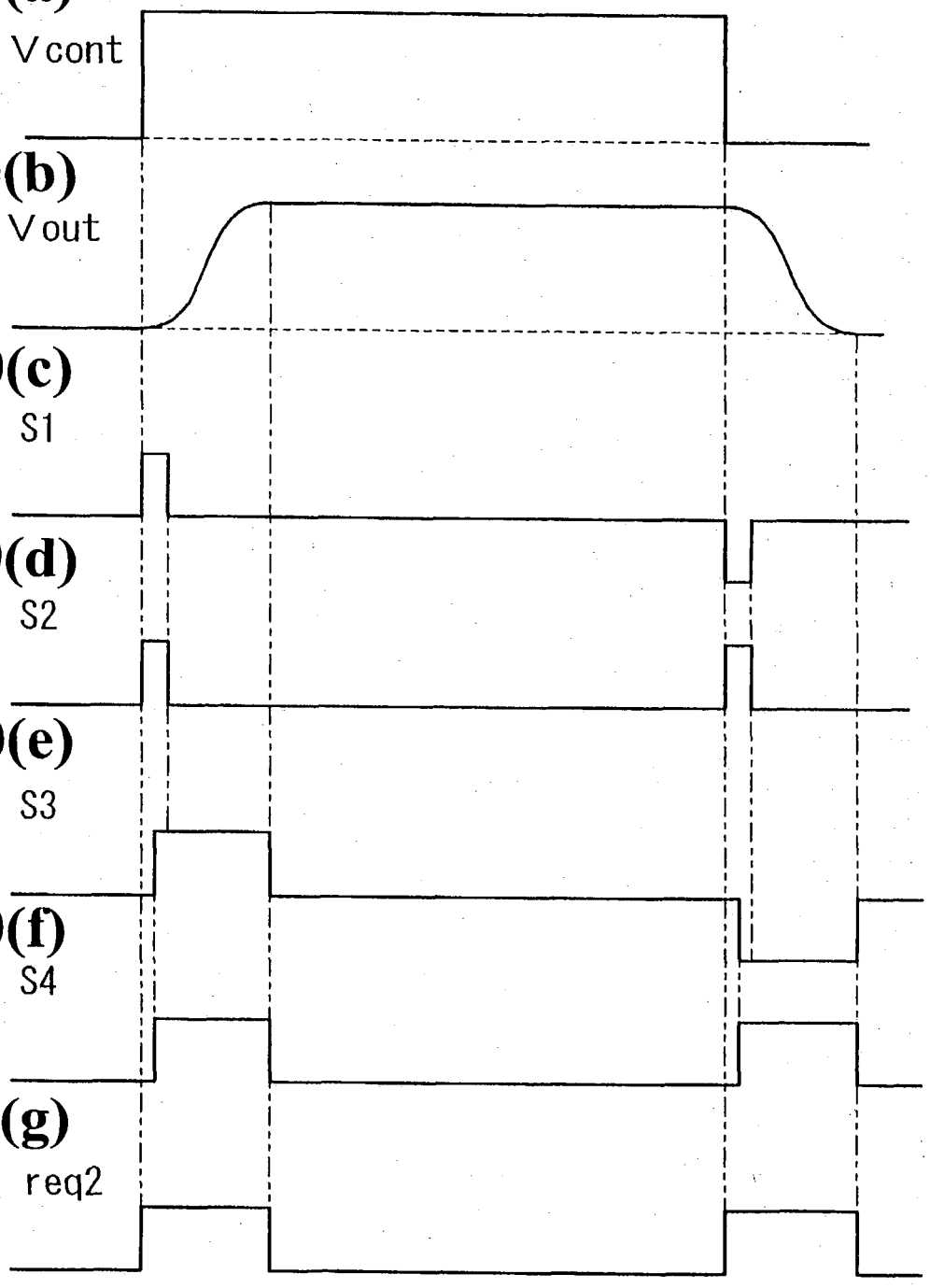


Fig. 11

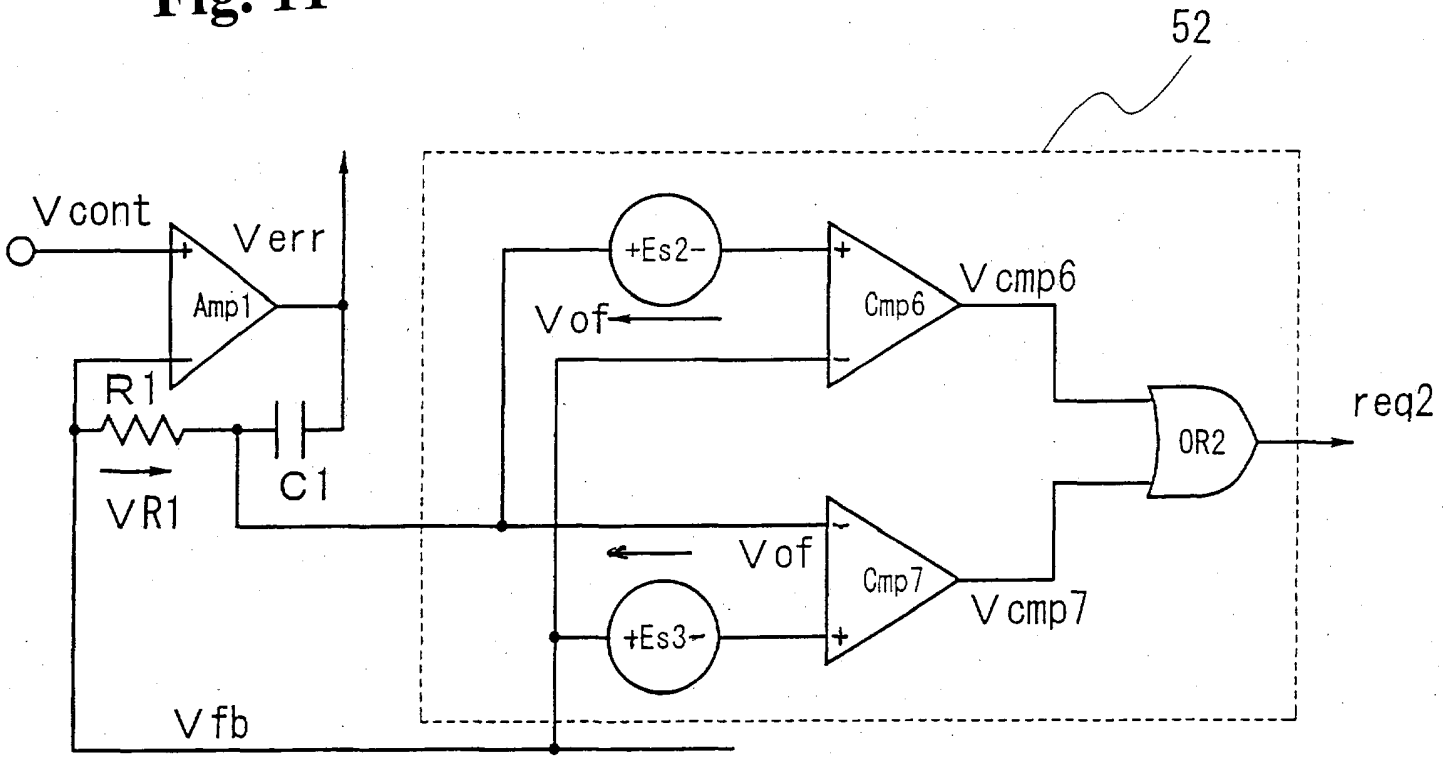

52
Vcont
Verr
Amp1
R1
VR1
C1
Vfb
+Es2-
Vof
Cmp6
Vcmp6
+Es3-
Vof
Cmp7
Vcmp7
OR2
req2

Fig. 12(a)

Fig. 12(b)

Fig. 12(c)

Fig. 12(d)

Fig. 12(e)

Fig. 12(f)

Fig. 12(g)

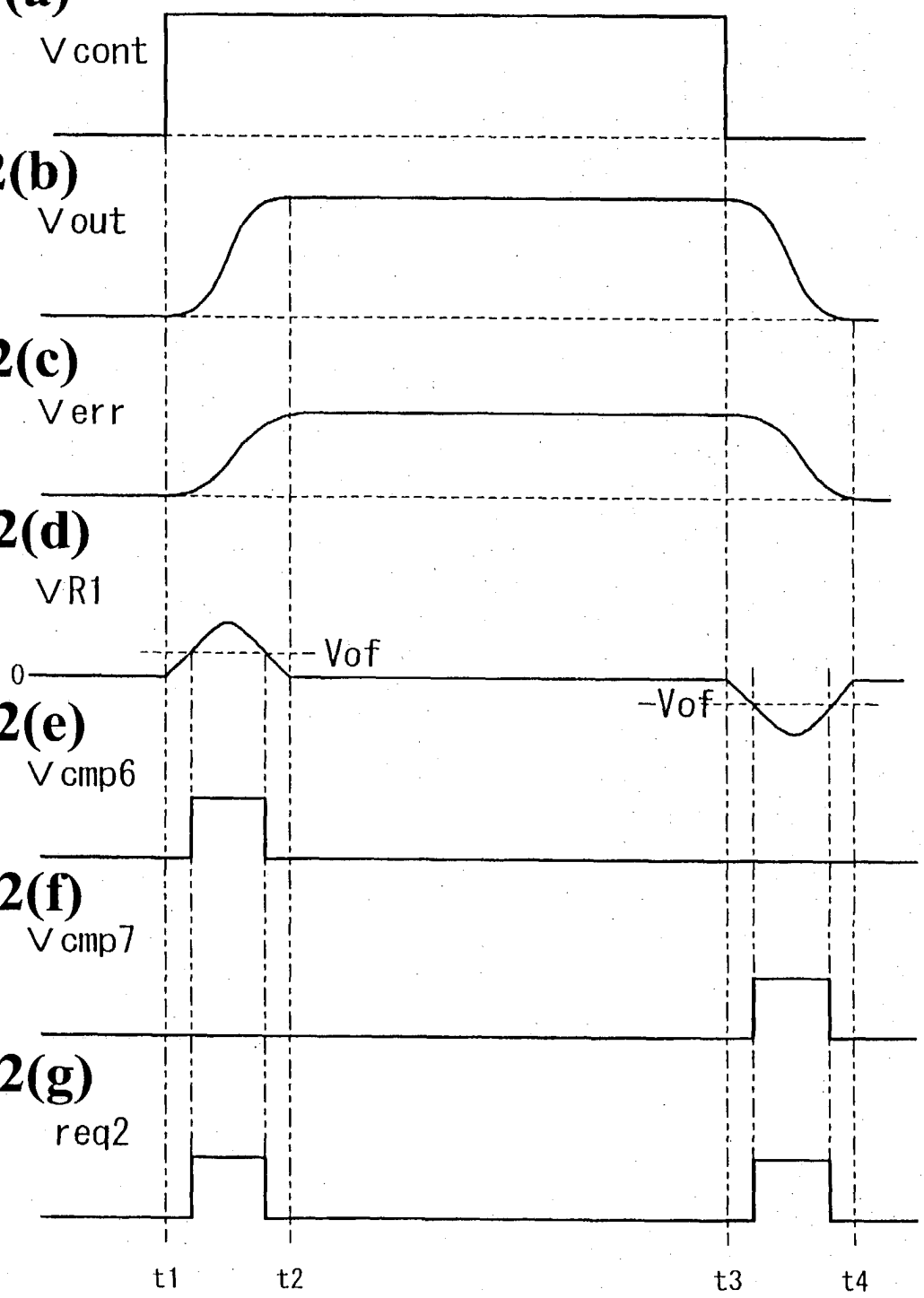


Fig. 13(a)

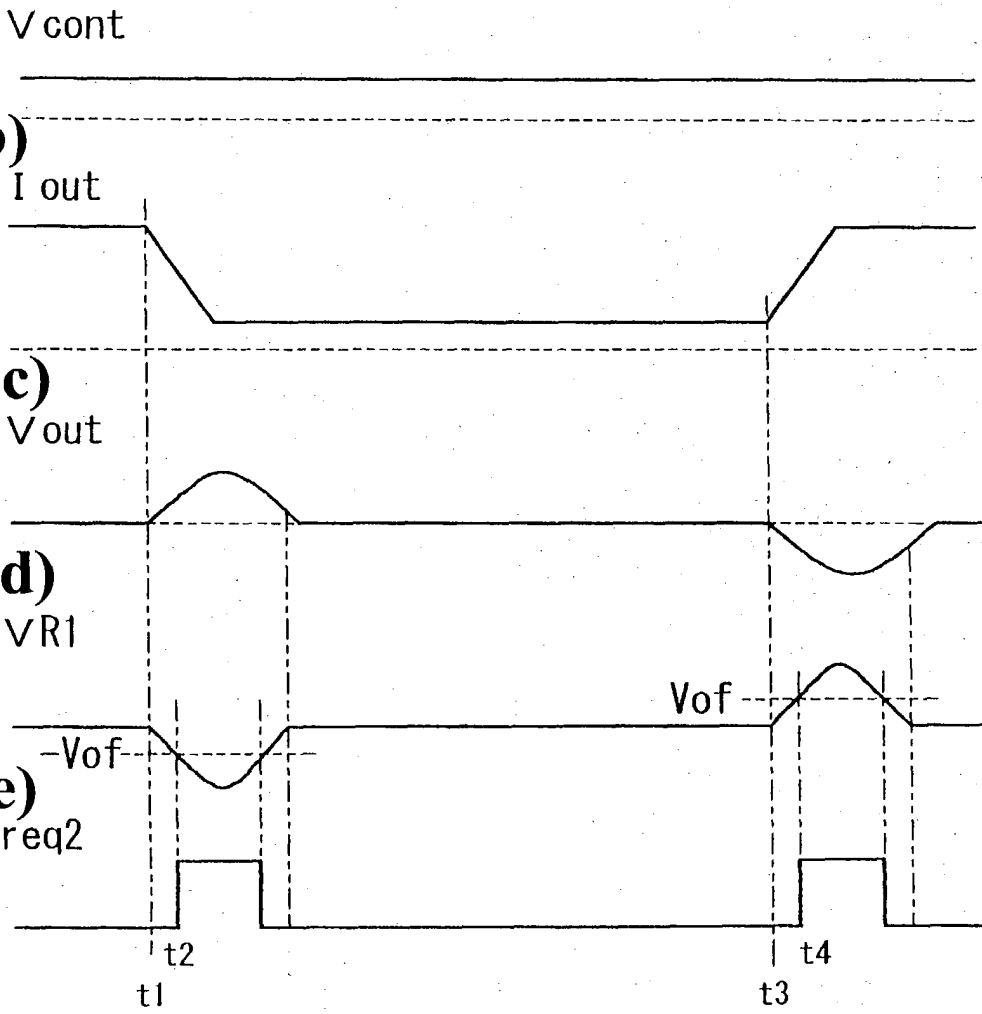


Fig. 13(b)

Fig. 13(c)

Fig. 13(d)

Fig. 13(e)

Fig. 14(a)

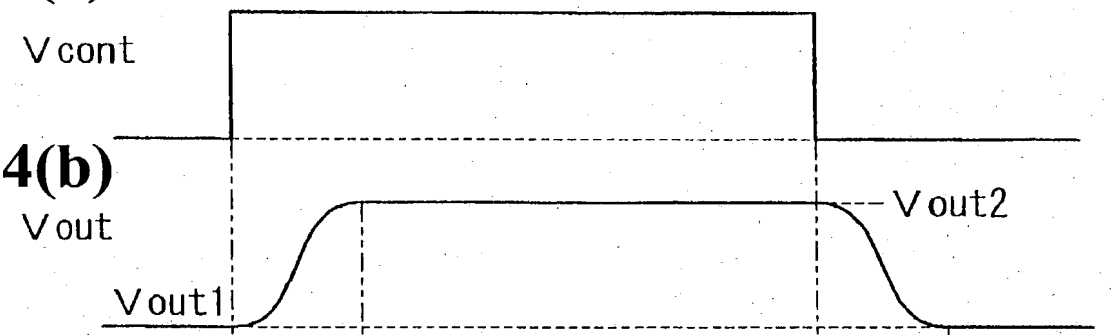


Fig. 14(b)

Fig. 14(c)

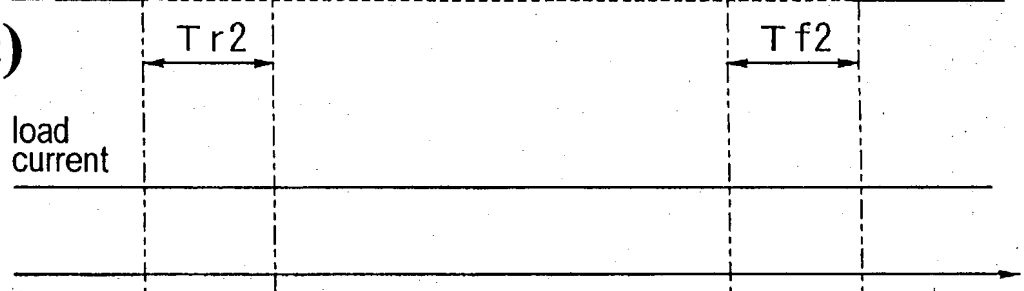


Fig. 14(d)

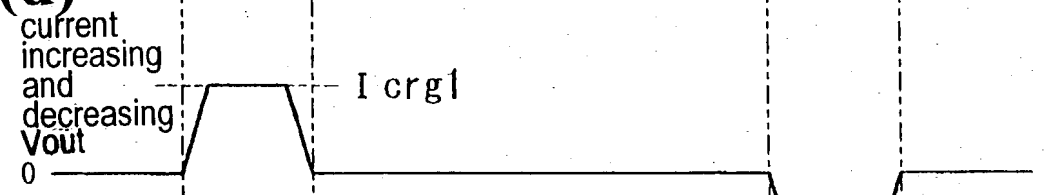


Fig. 14(e)

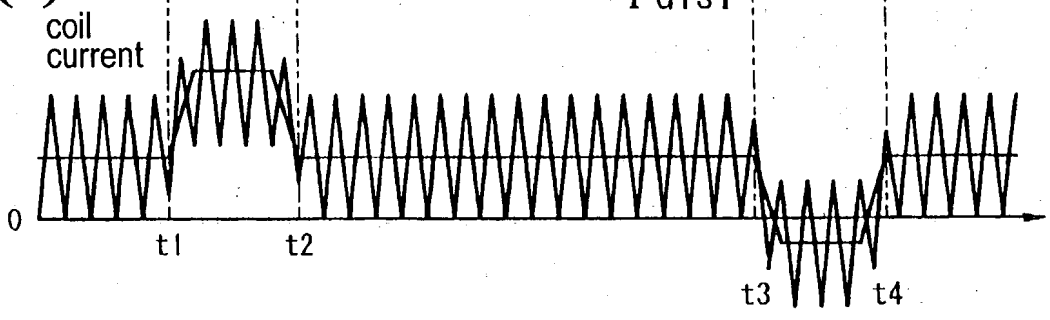


Fig. 15(a)

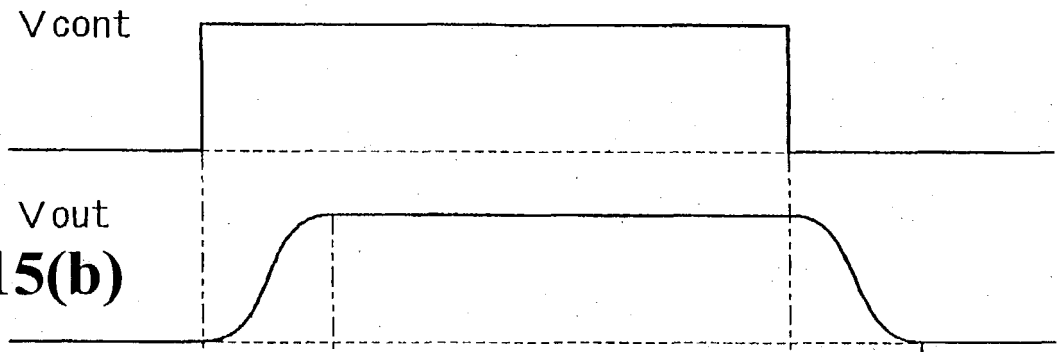


Fig. 15(b)

Fig. 15(c)

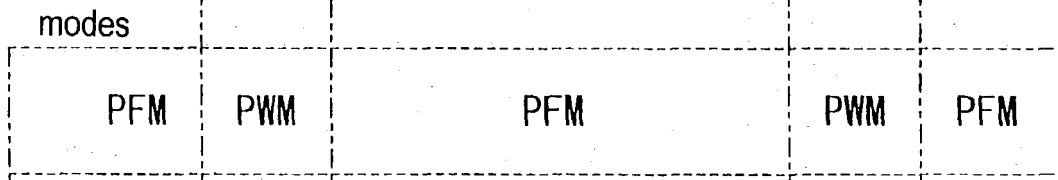


Fig. 15(d)

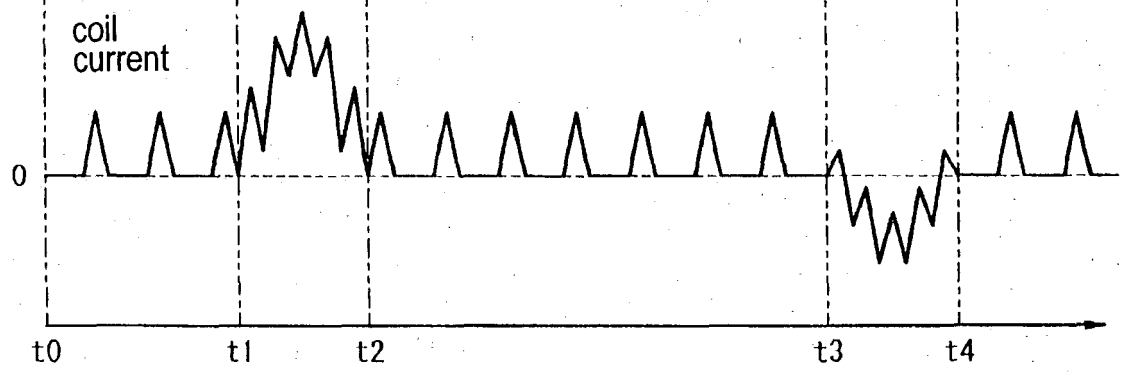


Fig. 16(a)

Fig. 16(b)

Fig. 16(c)

Fig. 16(d)

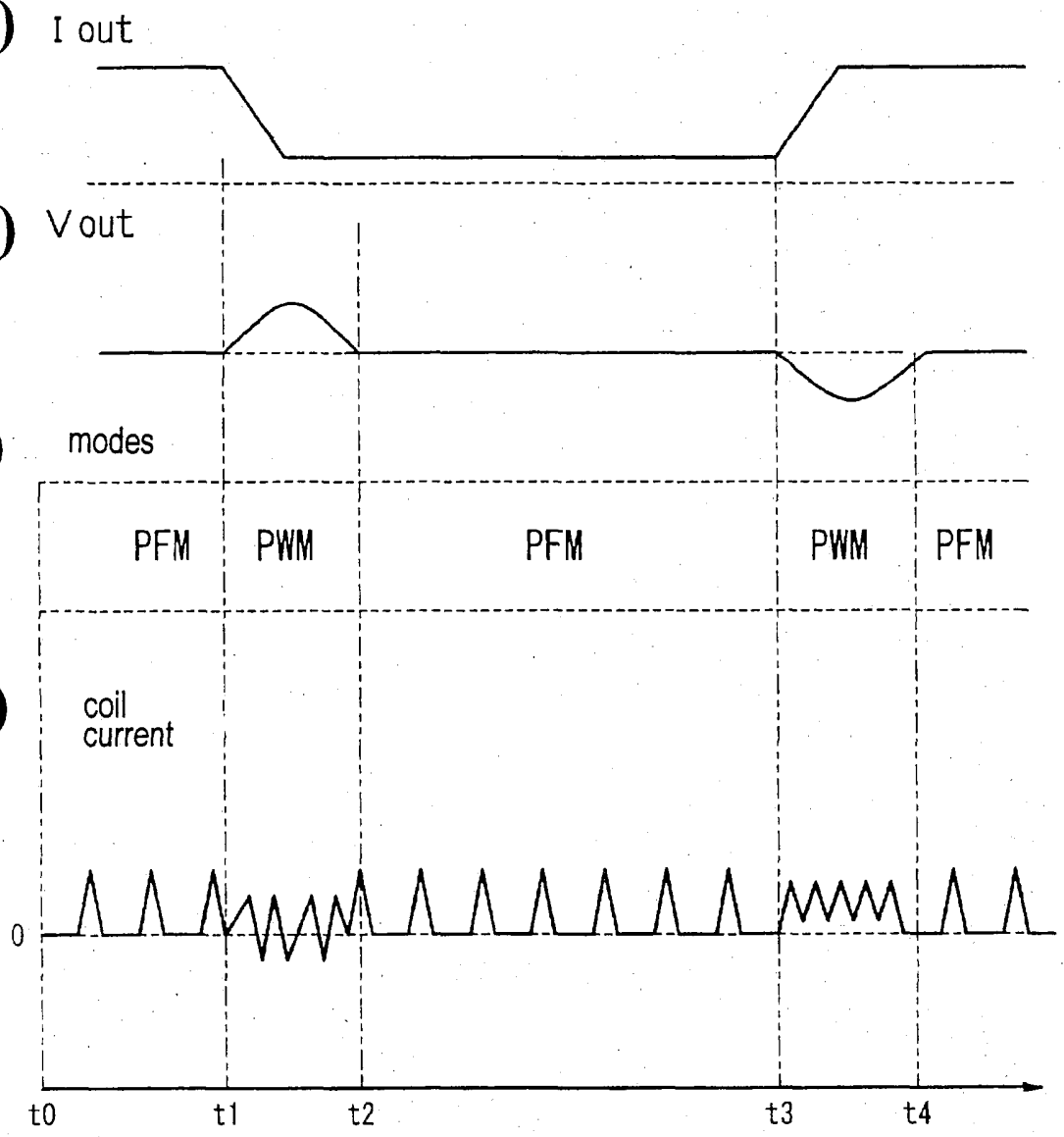


Fig. 17

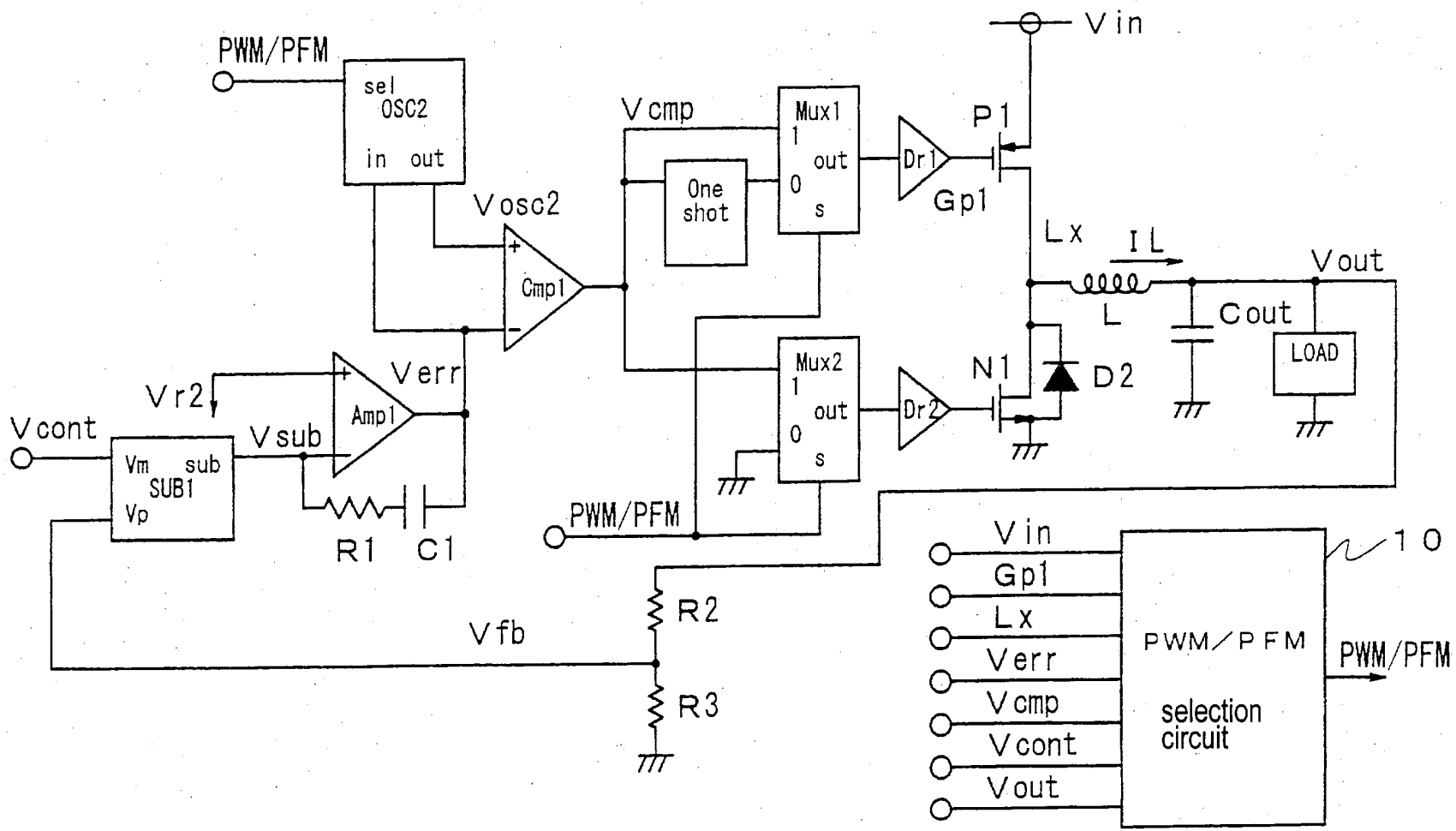

PWM/PFM
sel
OSC2
in out
Vosc2
Vcmp
One shot
Mux1
1
0
out
s
Dr1
P1
Gp1
Vin
Lx
IL
Vout
L
Cout
LOAD
Cmp1
Mux2
N1
D2
Dr2
Verr
Vr2
Amp1
Vcont
Vsub
Vm sub
SUB1
Vp
R1
C1
PWM/PFM
R2
Vfb
R3
Vin
Gp1
Lx
Verr
Vcmp
Vcont
Vout
PWM/PFM
selection
circuit
10

Fig. 18

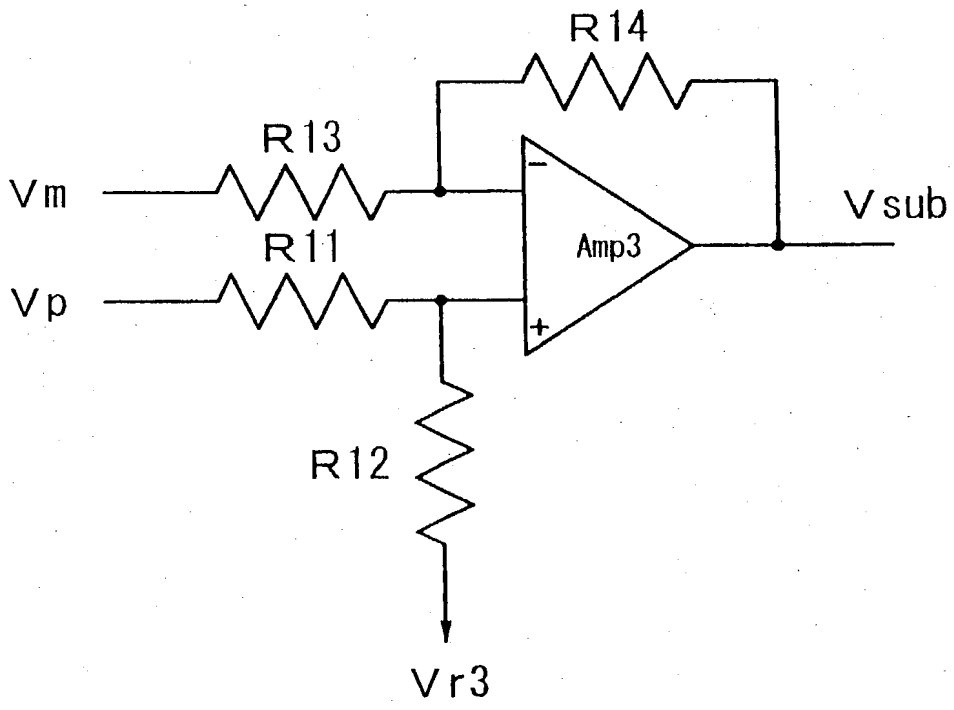


Fig. 19

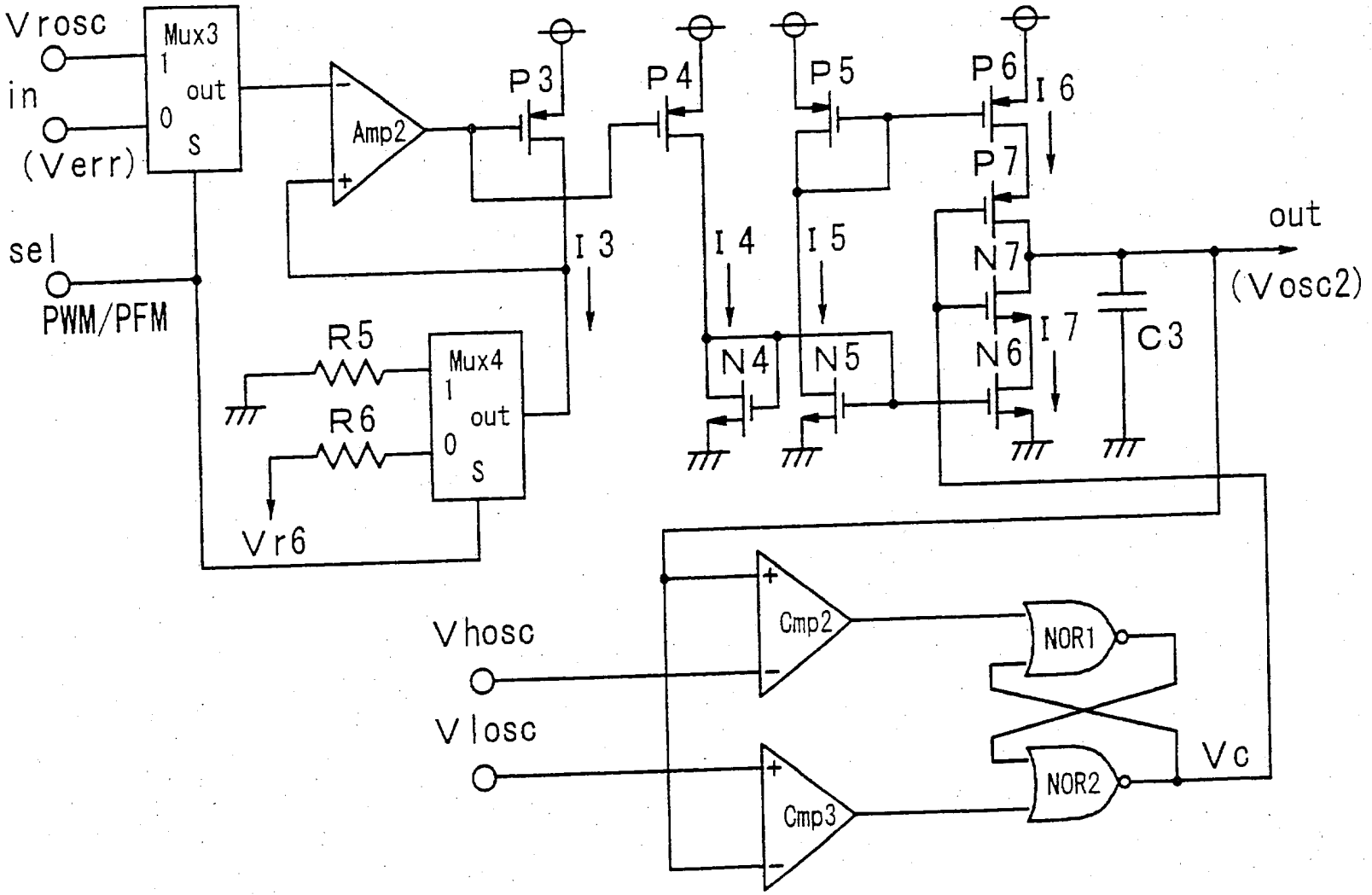

Vrosc
in
(Verr)
Mux3
1
0
out
S
Amp2
P3
P4
P5
P6
I6
P7
out
(Vosc2)
sel
PWM/PFM
I3
I4
I5
N7
N4
N5
N6
I7
C3
R5
R6
Mux4
Vr6
Vhosc
Vlosc
Cmp2
Cmp3
NOR1
NOR2
Vc

Fig. 20

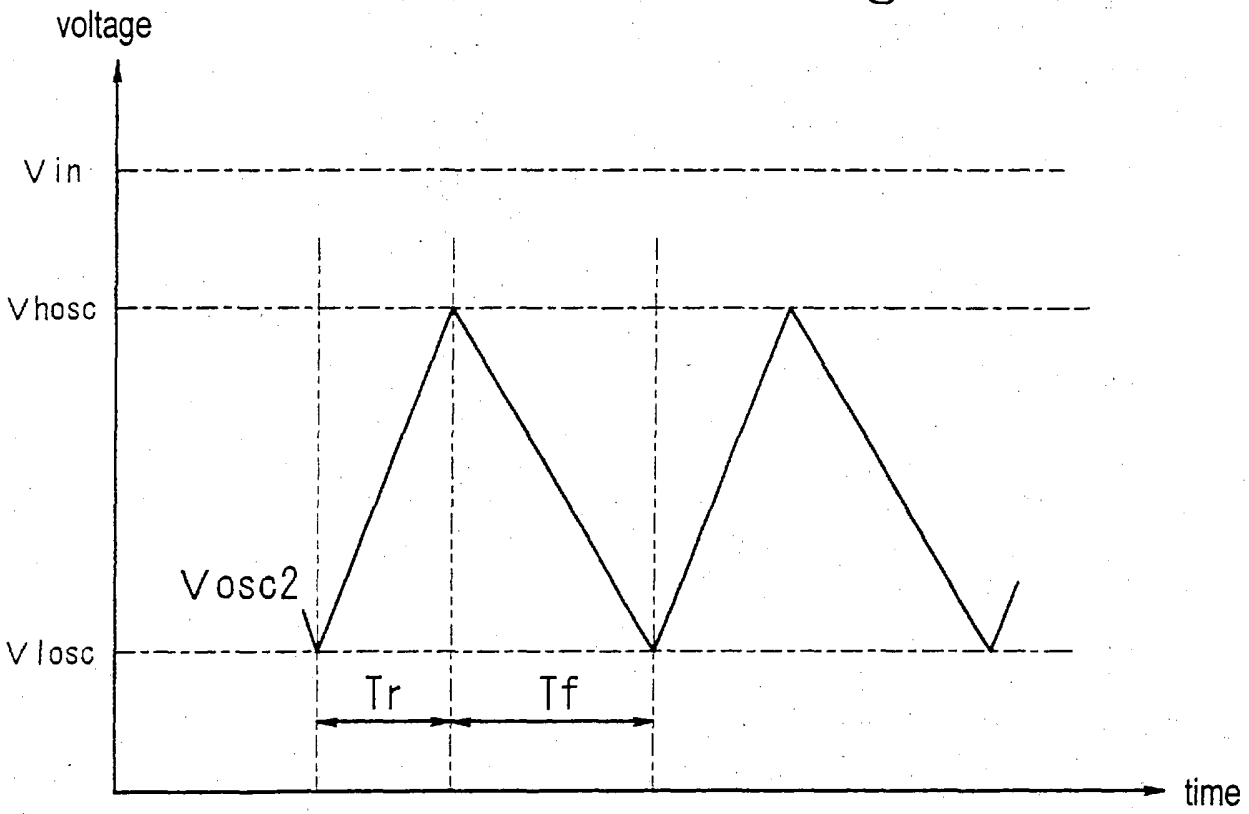


Fig. 21

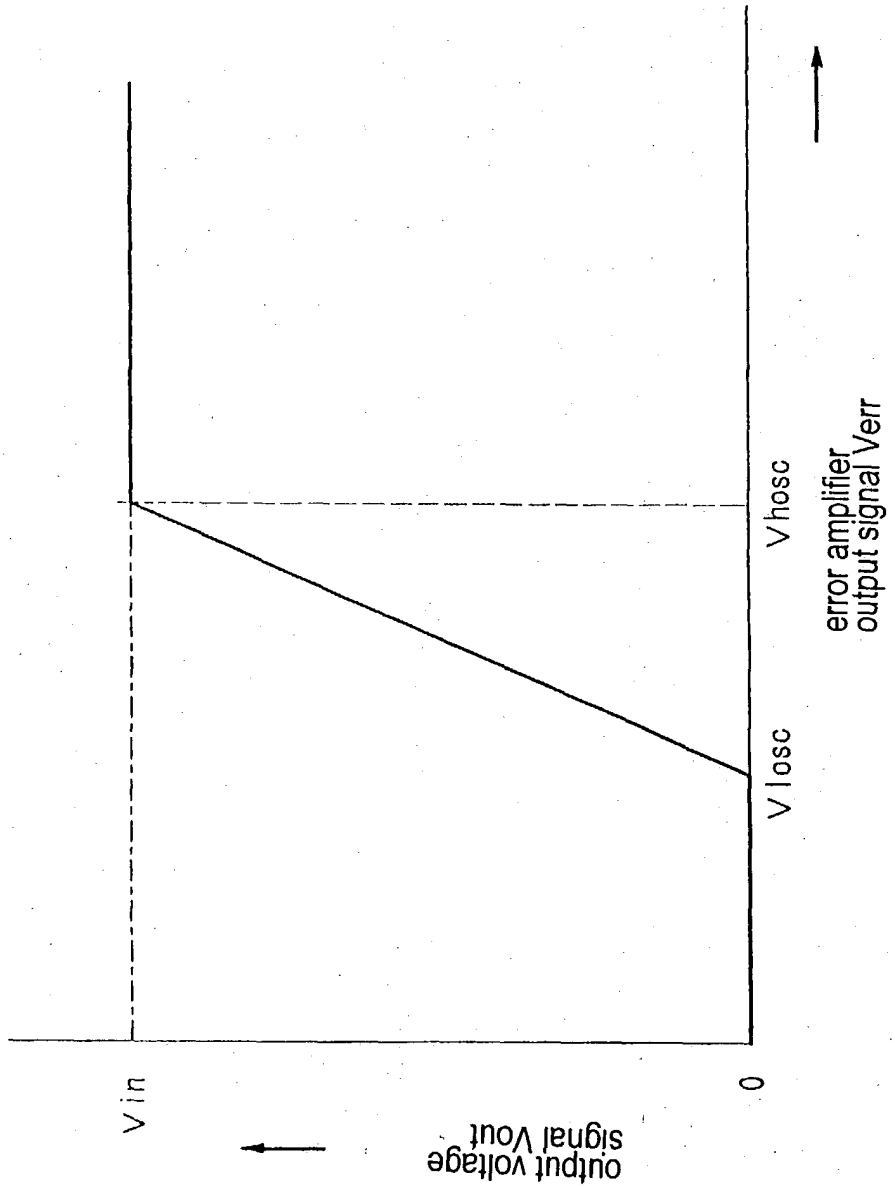

Vin
0
output voltage
signal Vout
V losc
Vhosc
error amplifier
output signal Verr

Fig. 22

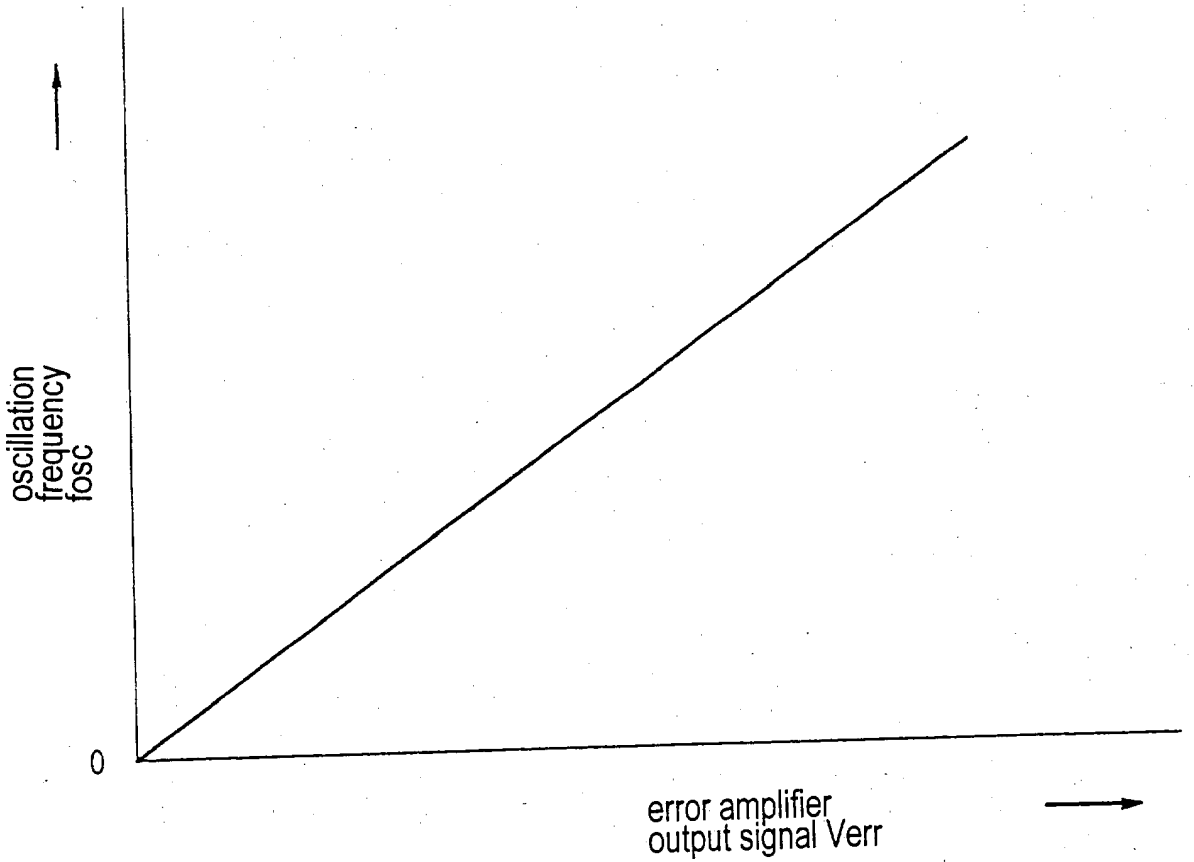

oscillation
frequency
fosc
0
error amplifier
output signal Verr

Fig. 23

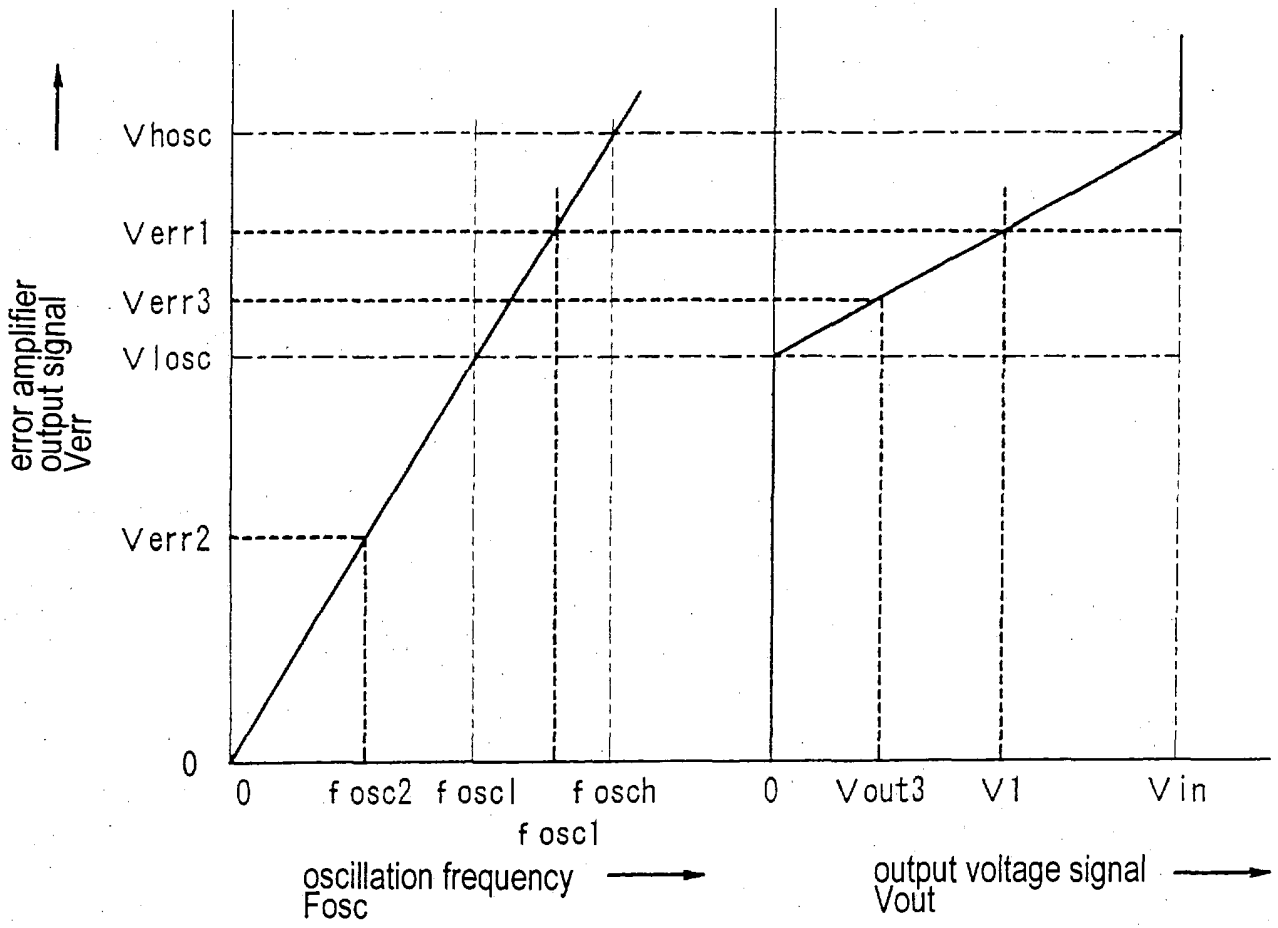

Vhosc
Verr1
Verr3
Vlosc
Verr2
0
error amplifier output signal Verr
0
f osc2
f oscl
f osch
f oscl
oscillation frequency Fosc
0
Vout3
V1
Vin
output voltage signal Vout

Fig. 24(a)

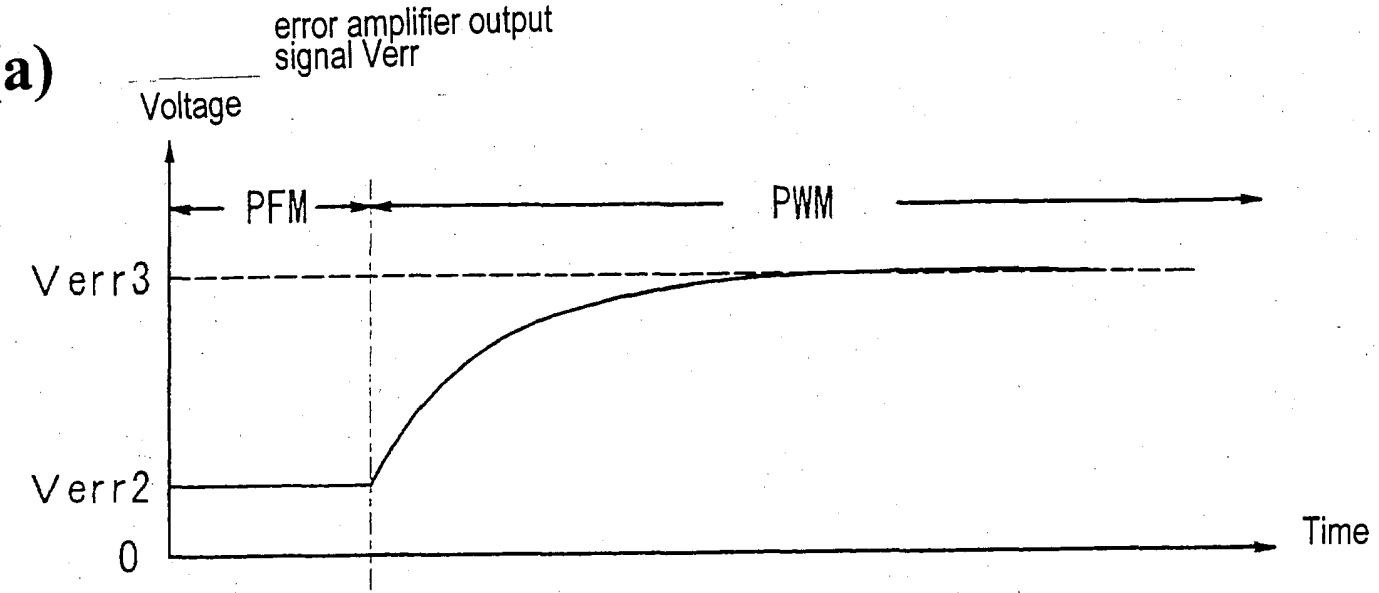


Fig. 24(b)

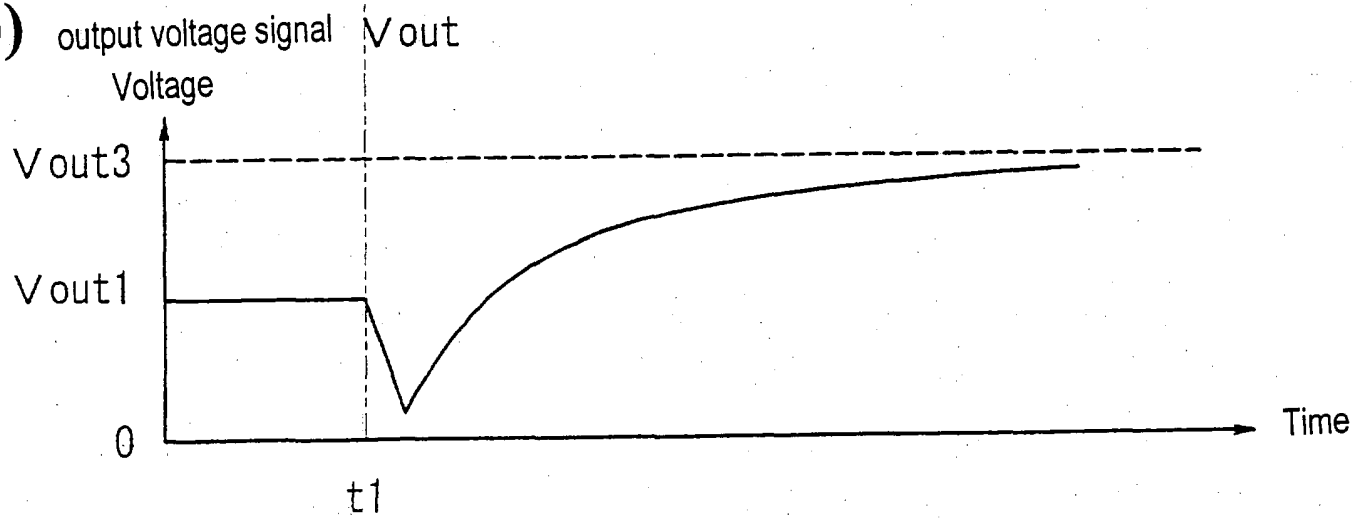


Fig. 25(a)

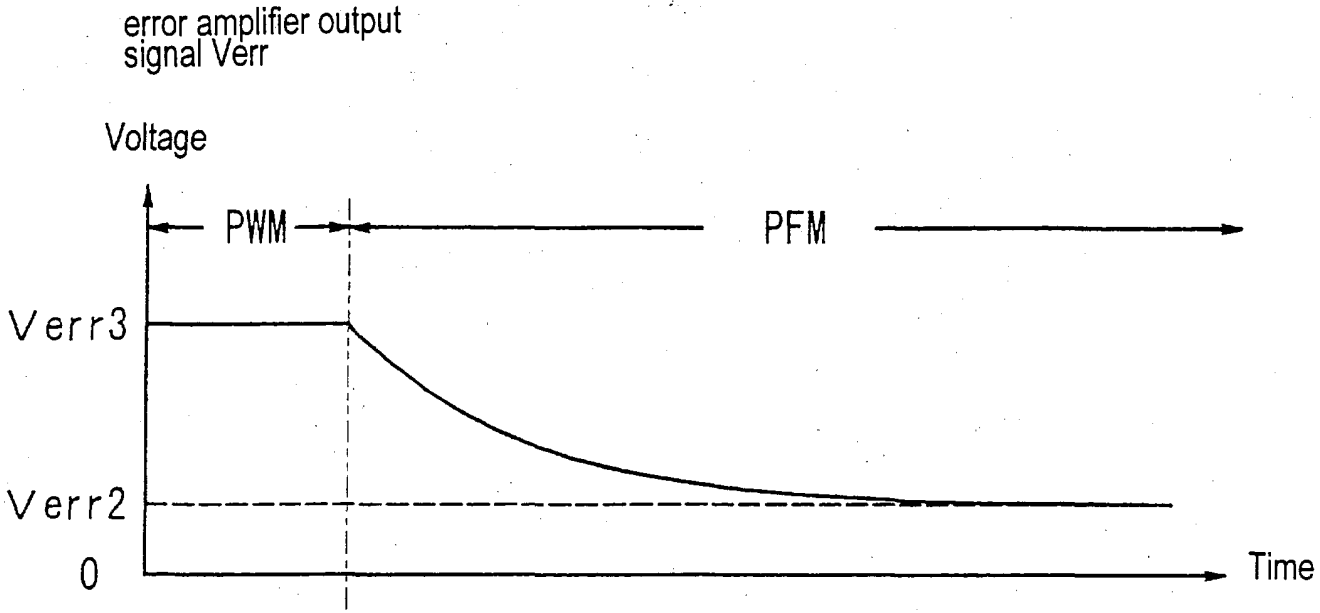


Fig. 25(b)

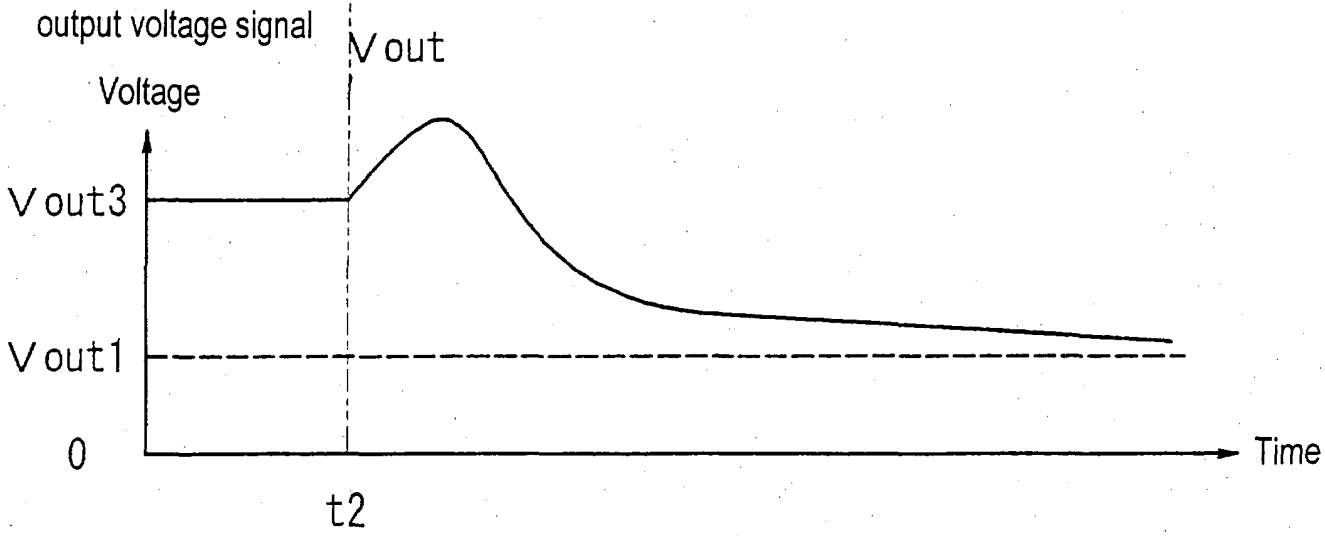


Fig. 26

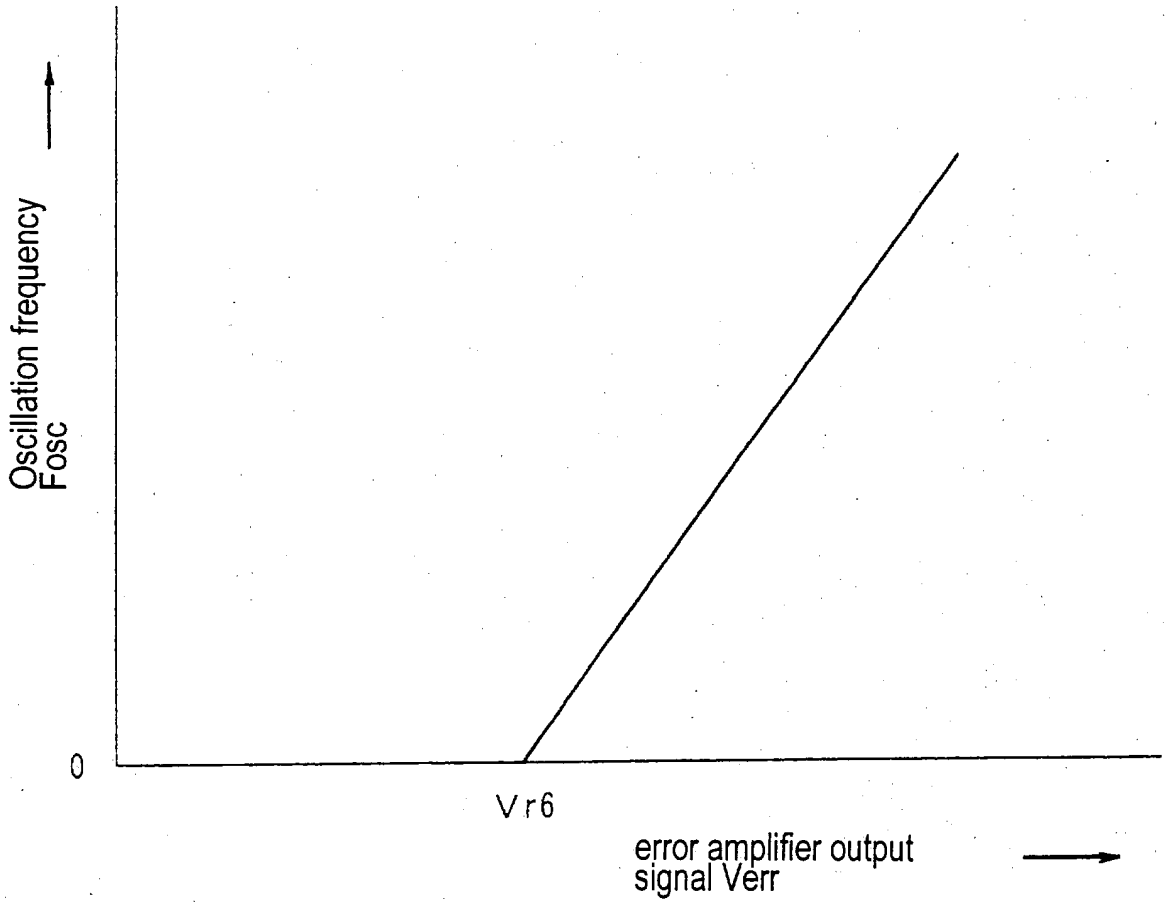

Oscillation frequency
Fosc
0
Vr6
error amplifier output
signal Verr

Fig. 27

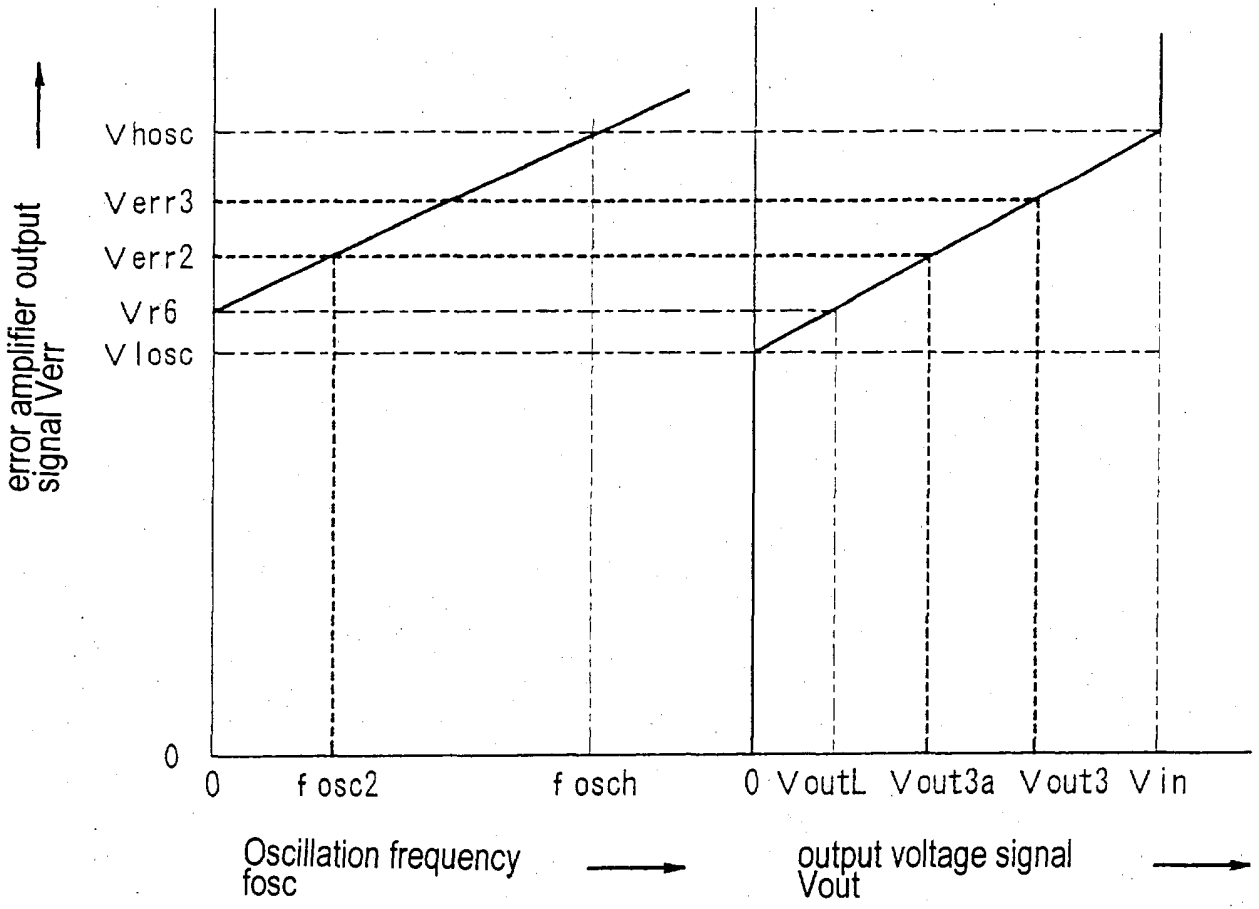

error amplifier output signal Verr
Vhosc
Verr3
Verr2
Vr6
Vlosc
0
0
f osc2
f osch
0
VoutL
Vout3a
Vout3
Vin
Oscillation frequency fosc
output voltage signal Vout

Fig. 28

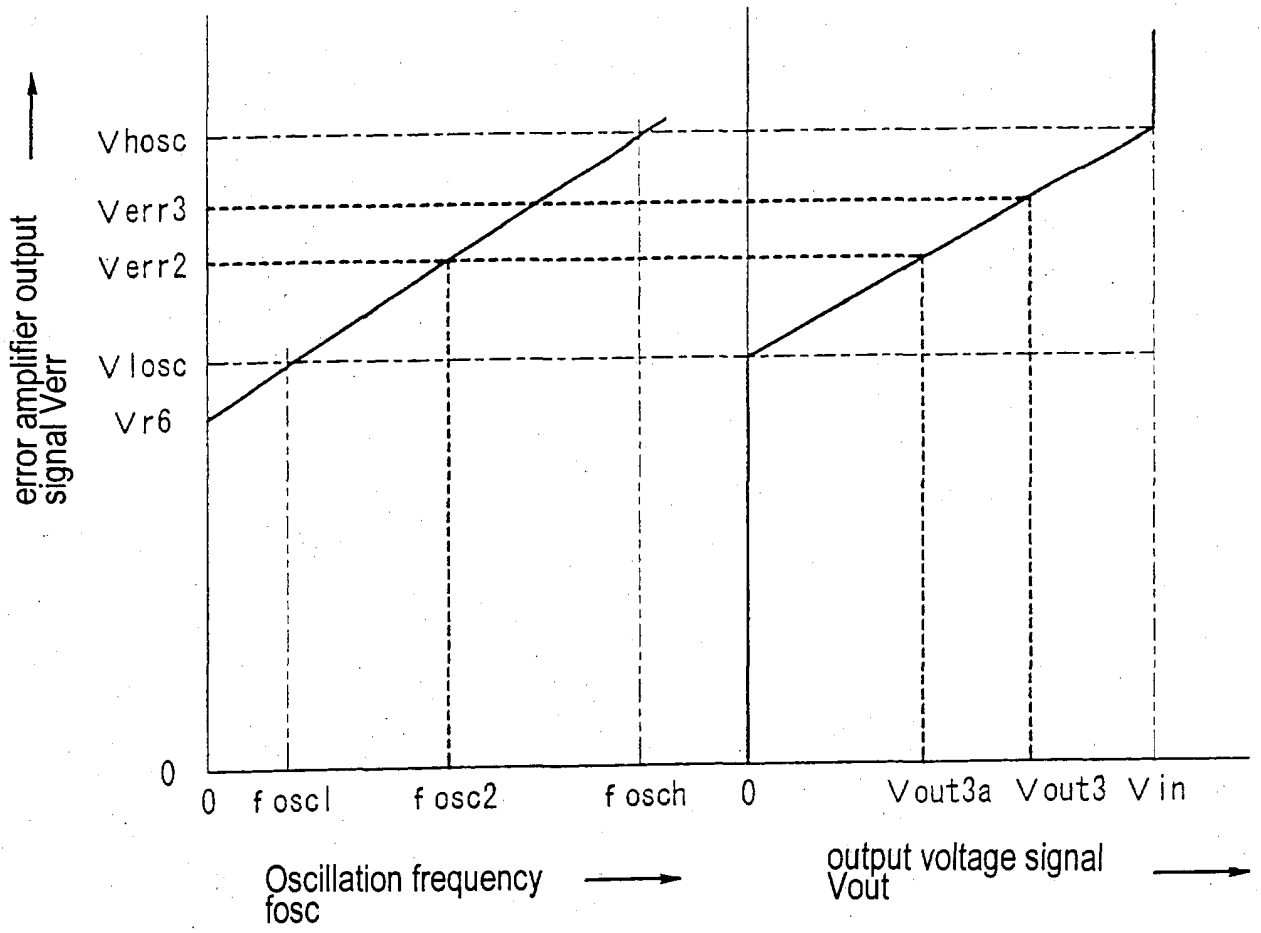

error amplifier output signal Verr
Vhosc
Verr3
Verr2
Vlosc
Vr6
0
0
f oscl
f osc2
f osch
0
Vout3a
Vout3
Vin
Oscillation frequency fosc
output voltage signal Vout

Fig. 29 Prior Art

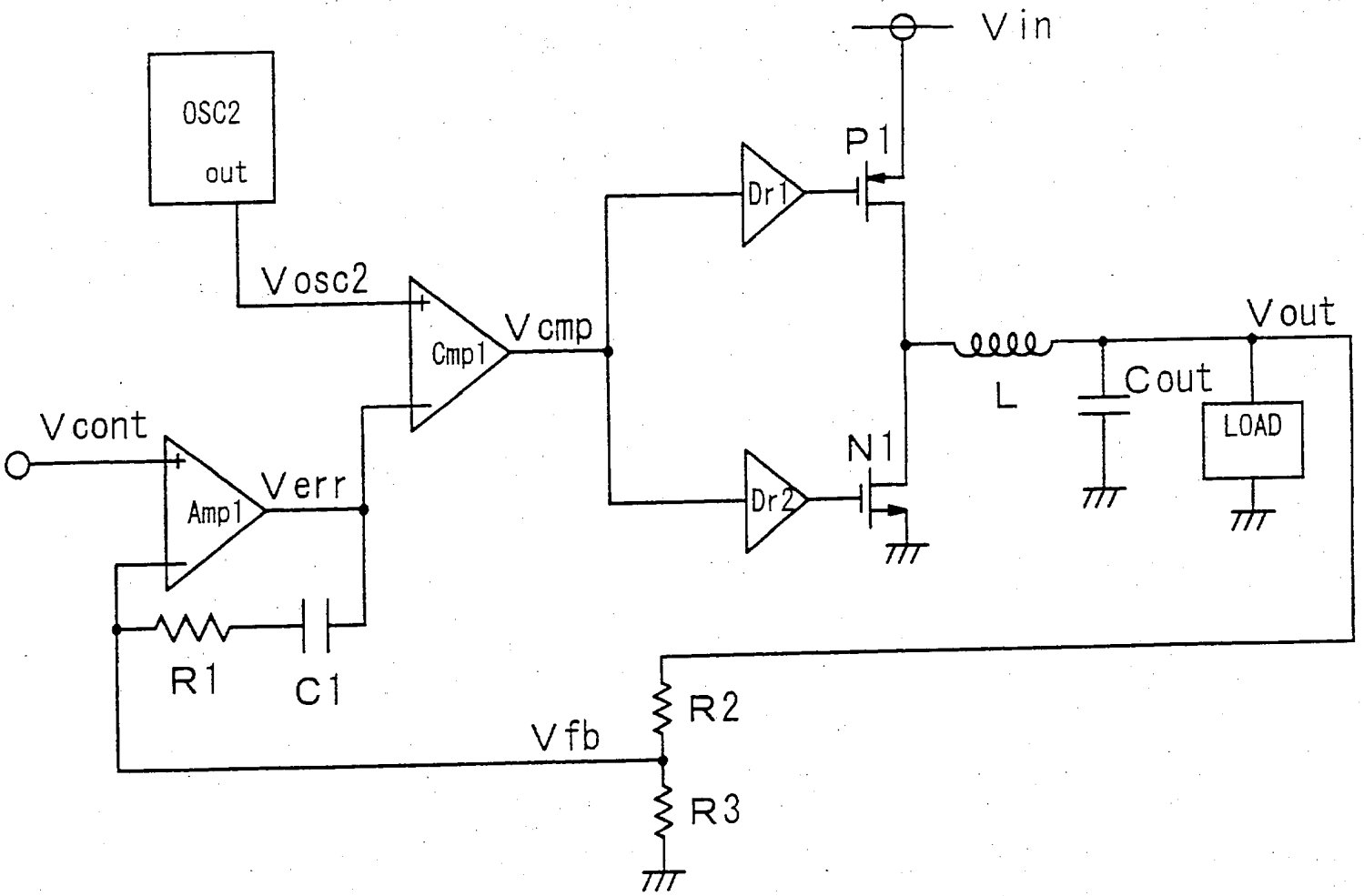


Fig. 30(a)
Prior Art

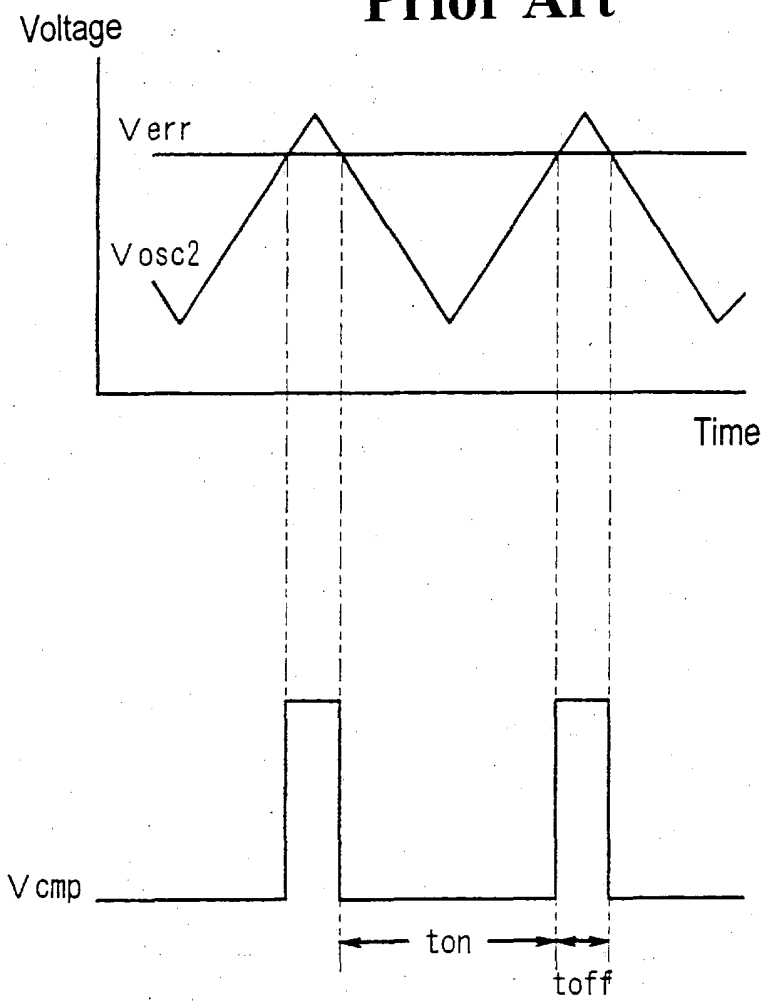


Fig. 30(b)
Prior Art

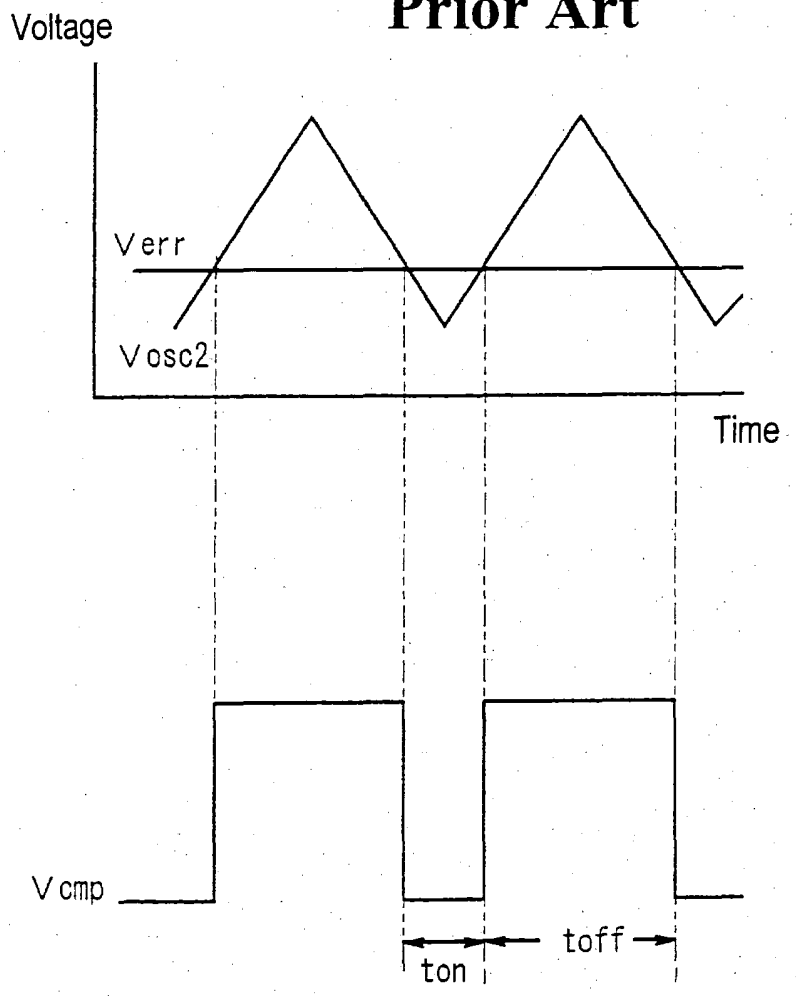


Fig. 31 Prior Art

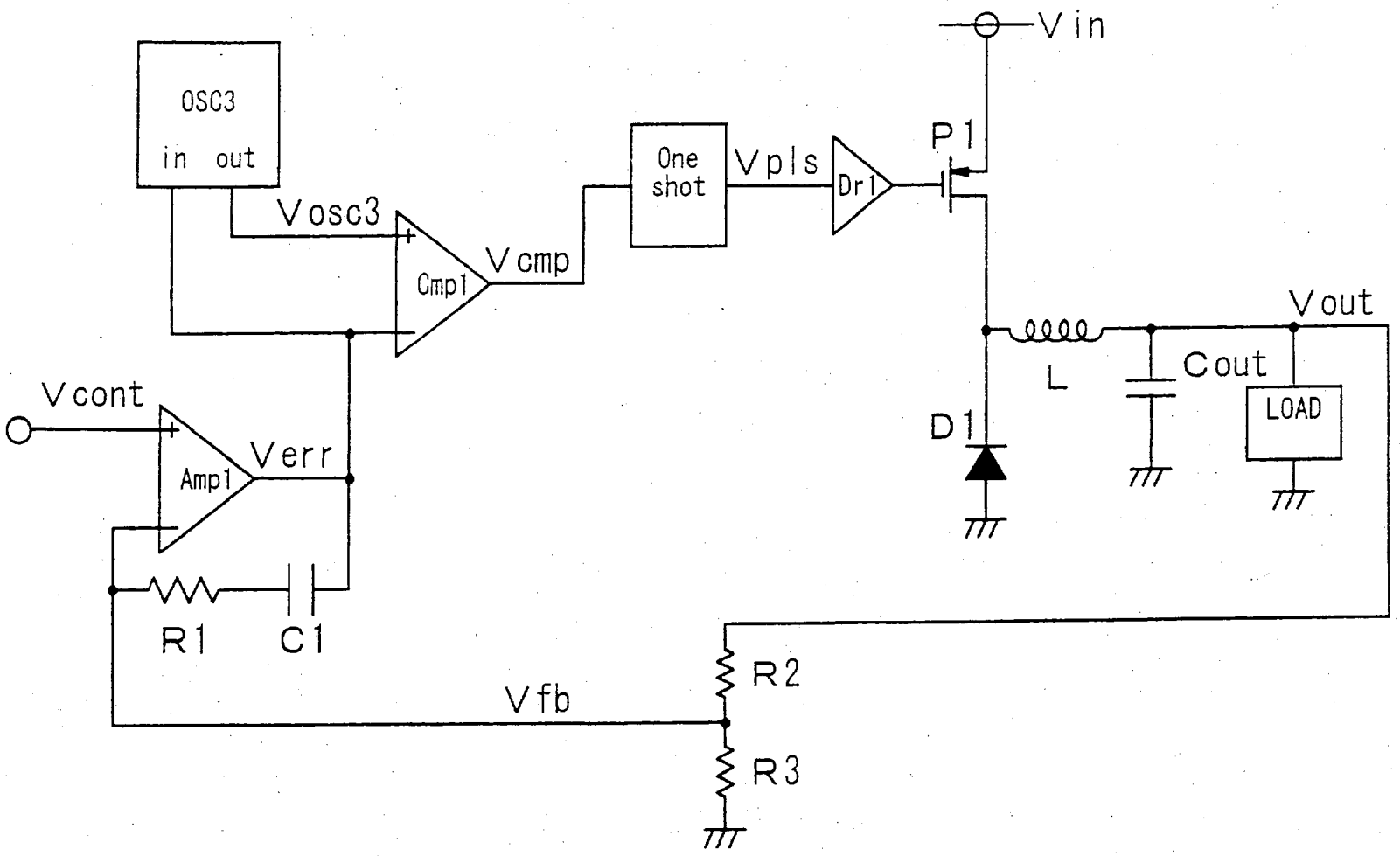


Fig. 32(a) Prior Art

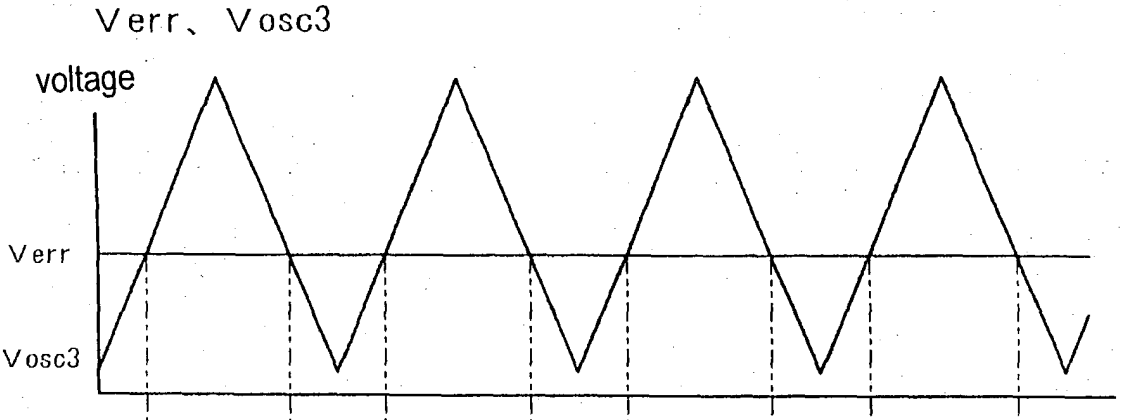


Fig. 32(b) Prior Art

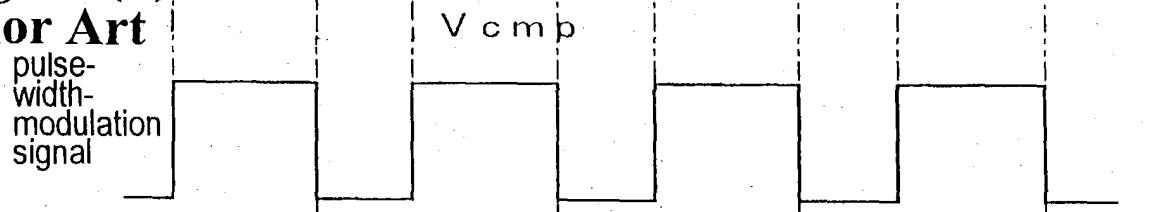


Fig. 32(c) Prior Art

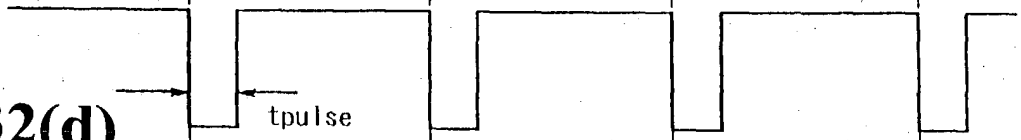


Fig. 32(d) Prior Art

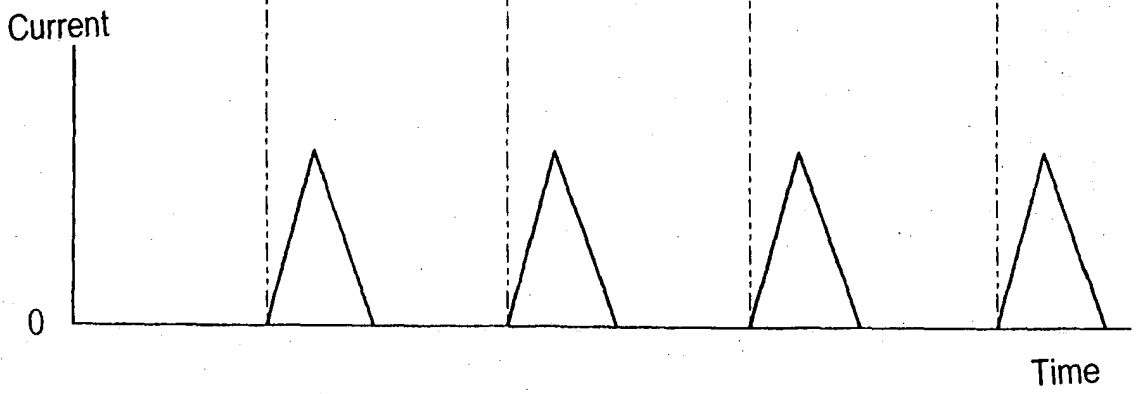


Fig. 33(a) Prior Art

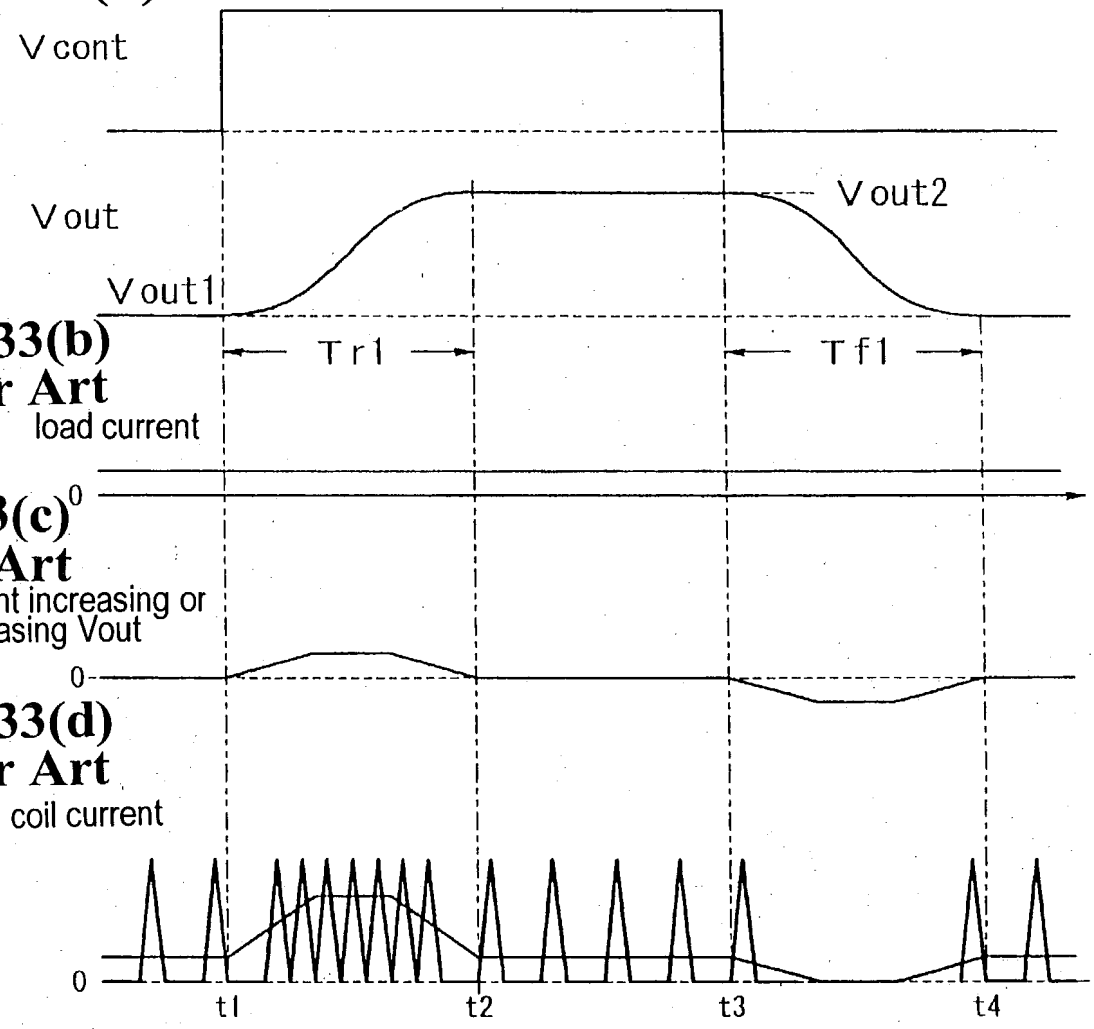


Fig. 33(b) Prior Art

Fig. 33(c) Prior Art

Fig. 33(d) Prior Art